4744

# SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 10/9/02 Serial # 10/043,946 Priority Application Date 12/18/00

Your Name M. Lewis Examiner # _____

AU 2882 Phone 305-3943 Room Plaza 3-3B07

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

10-09-02 P03:43 IN

**If submitting more than one search, please prioritize in order of need.**

**The EIC searcher normally will contact you before beginning a prior art search. If you would lik to sit with a searcher for an interactive search, please notify one of the searchers.**

**Where** have you searched so far on this case?
Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

**What** relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

**What** types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____
Secondary Refs ✓ Foreign Patents ___
Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-11 & 19-25

Problem: See Paragraph 2.

Solution: " " -3-6

Novelty in structure illustrated in the claims

| Staff Use Only | Type of Search | Vendors |
|---|---|---|
| Searcher: Derrick Brantley | Structure (#) | STN ✓ |
| Searcher Phone: | Bibliographic ✓ | Dialog ✓ |
| Searcher Location: STIC-EIC2800, CP4-9C18 | Litigation | Questel/Orbit |
| Date Searcher Picked Up: 10/9/02 | Fulltext | Lexis-Nexis |
| Date Completed: 10/10/02 | Patent Family | WWW/Internet |
| Searcher Prep/Rev Time: 25 | Other | Other |
| Online Time: 46 | | |

```
SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2002/Oct W1
         (c) 2002 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
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removal, customized scheduling. See HELP ALERT.
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removal, customized scheduling. See HELP ALERT.
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removal, customized scheduling. See HELP ALERT.
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         (c) 2002 ProQuest Info&Learning
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removal, customized scheduling.  See HELP ALERT.
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         (c) 2002 Elsevier Science Ltd.
  File 103:Energy SciTec  1974-2002/Sep B2
         (c) 2002 Contains copyrighted material
*File 103: For access restrictions see Help Restrict.
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| Set | Items | Description |
|---|---|---|
| S1 | 5 | AU=(PAEK, JONG OR PAEK, J OR PAEK JONG OR PAEK J) |
| S2 | 4869110 | (PACKAGE? OR ENCAS????? OR PROTECT? OR CASING OR CASE OR CAVITY OR ENCAPSUL? OR CAPSUL?) |
| S3 | 1737592 | IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT? ?)) OR (MICRO)(W)(CIRCUIT? ? OR CHIP? ? OR ELECTRONIC?) OR CHIP? ? OR MICROCIRCUIT? ? OR DIE? ? OR LOGIC(W) CIRCUIT? ? OR WAFER? ? OR MICROELECTRONIC? OR DICE |
| S4 | 72297 | CC=B2570 Semiconductor integrated circuits |
| S5 | 5451 | (CONTACT? OR BOND???)(2N)(PAD OR PADS OR BUMP OR BUMPS) |
| S6 | 194988 | (S3 OR S4) AND S2 |
| S7 | 1058 | S6 AND S5 |
| S8 | 683 | RD (unique items) |
| S9 | 4 | S8 AND (CONDUCT?)(W)(WIRE? ? OR LINE? ?) |
| S10 | 21 | S8 AND (ELECTRICAL?)(W)(CONNECT? OR JOIN?) |
| S11 | 0 | S8 AND (CONDUCTIVE)(W)(CONNECTOR? ?) |
| S12 | 229 | S8 AND LEAD? ? |
| S13 | 0 | S12 AND PADDLE |
| S14 | 4 | S12 AND PERIPHERAL |
| S15 | 13 | S8 AND PERIPHERAL |
| S16 | 0 | S12 AND PLURALITY |
| S17 | 0 | S8 AND PADDLE? ? |
| S18 | 0 | S5 AND (CONDUCT?)(W)(CONNECTOR? ?) |
| S19 | 80 | (CONDUCT?)(W)(CONNECTOR? ?) |
| S20 | 5 | (S3 OR S4) AND S19 |
| S21 | 68 | S12 AND (CONNECT??? OR JOIN???) |
| S22 | 19 | S21 AND ELECTRICAL? |
| S23 | 57 | S9 OR S10 OR S14 OR S15 OR S20 OR S22 |
| S24 | 57 | RD (unique items) |

1/3,AB/1 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci


09960368 Genuine Article#: 469RM Number of References: 14
Title: An estimation of traffic parameters for VBR services in ATM networks (ABSTRACT AVAILABLE)
Author(s): **Paek J**; Oh C (REPRINT) ; Kim K
Corporate Source: Kwang Ju Inst Sci & Technol,Dept Informat & Commun,Kwangju//South Korea/ (REPRINT); Kwang Ju Inst Sci & Technol,Dept Informat & Commun,Kwangju//South Korea/
Journal: COMPUTER COMMUNICATIONS, 2001, V24, N14 (SEP 15), P1380-1389
ISSN: 0140-3664 Publication date: 20010915
Publisher: ELSEVIER SCIENCE BV, PO BOX 211, 1000 AE AMSTERDAM, NETHERLANDS
Language: English Document Type: ARTICLE
Abstract: In order to guarantee a proper operation of both UPC/NPC and CAC functions in ATM networks, the intrinsic traffic characteristics of connections should first be adequately described by a set of standardized traffic parameters. The most significant traffic descriptors for the VBR service are SCR (Sustainable Cell Rate) and MBS (Maximum Burst Size). In this paper, we work on traffic parameters estimation from VBR source modeling in ATM networks. We propose a new method of traffic parameters estimation from the VBR ON/OFF source model, which satisfies the quality of service (QoS) requirements with the least cost. (C) 2001 Elsevier Science B.V. All rights reserved.

1/3,AB/2 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci


06015555 Genuine Article#: XP277 Number of References: 9
Title: Raman spectroscopic study on the modification of the mesogenic unit in a liquid crystalline oligomer under two different conditions
Author(s): Yu SC (REPRINT) ; **Paek J**; Yu KH; Ko SB; Cho IH; Lee M
Corporate Source: KUNSAN NATL UNIV,DEPT CHEM/CHONJU 573701//SOUTH KOREA/ (REPRINT); CHONBUK NATL UNIV,DEPT CHEM/CHONJU 561756//SOUTH KOREA/; YONSEI UNIV,DEPT CHEM/SEOUL 120749//SOUTH KOREA/
Journal: BULLETIN OF THE KOREAN CHEMICAL SOCIETY, 1997, V18, N7 (JUL 20), P 773-775
ISSN: 0253-2964 Publication date: 19970720
Publisher: KOREAN CHEMICAL SOC, 635-4 YEOGSAM-DONG, KANGNAM-GU, SEOUL 135-703, SOUTH KOREA
Language: English Document Type: ARTICLE

1/3,AB/3 (Item 3 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci


04818905 Genuine Article#: UK025 Number of References: 19
Title: VENTILATION EFFECTS ON MINERALIZATION AND VOLATILIZATION OF NAPHTHALENE IN A GASOLINE-CONTAMINATED SUBSURFACE SOIL (Abstract Available)
Author(s): HICKEY WJ; **PAEK J**

Corporate Source: UNIV WISCONSIN,DEPT SOIL SCI,1525 OBSERV DR/MADISON//WI/53706
Journal: CHEMOSPHERE, 1996, V32, N8 (APR), P1655-1667
ISSN: 0045-6535
Language: ENGLISH Document Type: ARTICLE
Abstract: Soil ventilation is widely used to promote in situ soil bioremediation at leaking underground storage tank sites. Effects of this process on microbial activity, however, are ill-defined. In this study, biodegradation and volatilization of a model fuel hydrocarbon ([C-14]naphthalene) in a gasoline-contaminated soil was determined in columns that were either intermittently or continuously ventilated at a low air-flow rate. With continuous ventilation, volatilization was extensive (up to 38.8%) and mineralization relatively minor (10.4%). Intermittent ventilation decreased volatilization ten-fold but also reduced mineralization to negligible levels. Compared to the continuously aerated columns, the intermittently vented soil had significant microbial population reductions, lower CO2 production, and higher residual gasoline. These results indicated that the ineffectiveness of intermittent ventilation for stimulating biodegradation could be attributed to its failure to reduce gasoline residues to sub-inhibitory levels. (C) 1996 Elsevier Science Ltd.

1/3,AB/4 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal


15341412 PASCAL No.: 02-0028104
An estimation of traffic parameters for VBR services in ATM networks
**PAEK J**; OH C; KIM K
Dept. of Info. and Communications Kwang-Ju Inst. of Sci. and Technol., Kwangju, Korea, Republic of
Journal: Computer Communications, 2001, 24 (14) 1380-1389
Language: English
In order to guarantee a proper operation of both UPC/NPC and CAC functions in ATM networks, the intrinsic traffic characteristics of connections should first be adequately described by a set of standardized traffic parameters. The most significant traffic descriptors for the VBR service are SCR (Sustainable Cell Rate) and MBS (Maximum Burst Size). In this paper, we work on traffic parameters estimation from VBR source modeling in ATM networks. We propose a new method of traffic parameters estimation from the VBR ON/OFF source model, which satisfies the quality of service (QoS) requirements with the least cost. 

1/3,AB/5 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal


08429417 PASCAL No.: 88-0430304
Cortical glucose metabolic rate correlates of abstract reasoning and attention studied with positron emission tomography
HAIER R J; SIEGEL B V JR; NUECHTERLEIN K H; HAZLETT E; WU J C; **PAEK J**; BROWNING H L; BUCHSBAUM M S
Univ. California, dep. psychiatry, Irvine CA 92717, USA
Journal: Intelligence (Norwood), 1988, 12 (2) 199-217

Language: ENGLISH
Etude examinant l'utilisation du glucose cerebral local pendant la resolution d'une epreuve de raisonnement abstrait par 30 jeunes adultes

24/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC


7411421 INSPEC Abstract Number: B2002-11-0170J-168
Title: CAD design for area pad transformation
Author(s): Yu-Jung Huang; Ching-Mai Ko; Shen-Li Fu
Author Affiliation: Dept. of Electron. Eng., I-Shou Univ., Kaohsiung, Taiwan
Conference Title: Proceedings 2001 International Symposium on Microelectronics (SPIE Vol.4587) p.610-15
Publisher: IMAPS - Int. Microelectron. & Packaging Soc, Washington, DC, USA
Publication Date: 2001 Country of Publication: USA xix+782 pp.
ISBN: 0 930815 64 5 Material Identity Number: XX-2002-00865
Conference Title: 2001 International Symposium on Microelectronics
Conference Sponsor: IMAPS - Int. Microelectron. & Packaging Soc
Conference Date: 9-11 Oct. 2001 Conference Location: Baltimore, MD, USA
Language: English
Abstract: As the demand for smaller, lighter, power efficient devices grows, the area array bonding technology are becoming more important for high pin count and high performance **packages**. Ball grid arrays (BGA) and **chip** scale **packages** (CSP) technologies are a major factor in the miniaturization and functionality of todays computing and communication products. However, the majority of existing **ICs** are usually designed in a **peripheral** format for wire bonding. Due to area array bonding for bare **die** becomes more prevalent, it is important to have the automatic design methodology for the **peripheral bond pads** to be relocated to area-array format. In this paper, we describe the methodology to solve the problem of redistributing from **bond pads** on periphery of the **IC** to area array of the solder bumps. Several computer aided design cases of the conversion technique from periphery wire-**bond pads** to an area array of pads are presented.
Subfile: B


24/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC


7411358 INSPEC Abstract Number: B2002-11-0170J-141
Title: Indium **bump bonding** for cryogenic applications
Author(s): Keeney, A.C.; Lee, D.M.; Lehtonen, S.J.; Francomacaro, A.S.
Author Affiliation: Appl. Phys. Lab., Johns Hopkins Univ., Laurel, MD, USA
Conference Title: Proceedings 2001 International Symposium on Microelectronics (SPIE Vol.4587) p.106-10
Publisher: IMAPS - Int. Microelectron. & Packaging Soc, Washington, DC, USA
Publication Date: 2001 Country of Publication: USA xix+782 pp.
ISBN: 0 930815 64 5 Material Identity Number: XX-2002-00865
Conference Title: 2001 International Symposium on Microelectronics
Conference Sponsor: IMAPS - Int. Microelectron. & Packaging Soc

Conference Date: 9-11 Oct. 2001 Conference Location: Baltimore, MD, USA
Language: English
Abstract: The growth of cryogenic applications for high performance electronic assemblies such as advanced imaging detectors and high speed computing systems is placing greater demands on the electronic packaging employed. With the temperature in which these electronic assemblies operate nearing zero kelvin, the packaging must be efficient and robust, and the materials utilized should possess super-conducting properties. In addition, the interconnect bonding metal must remain ductile in order to maintain good **electrical connection**. The Applied Physics Laboratory has developed a unique indium bump-plating process for creating the pad geometries needed for flip **chip** assembly techniques. Once the **die** involved were bump-plated, a flip **chip** bonding process was characterized for interconnecting large area **die** with over 4000 electrical contacts. The interconnects were then tested for resistance and reliability. The processes for forming the **bumps** and **bonding** the **die** is presented, along with electrical test data.
Subfile: B


24/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC


7307164 INSPEC Abstract Number: B2002-08-2240-008
Title: Fluxing for flip **chip** assembly - effect of bump damage
Author(s): Mahalingam, S.; Ji Hyon Mun; Prats, A.; Blass, D.; Srihari, K.
Author Affiliation: Dept. of Syst. Sci. & Ind. Eng., Binghamton Univ., NY, USA
Conference Title: Advances in Electronic Materials and Packaging 2001 (Cat. No.01EX506) p.135-8
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA xviii+449 pp.
ISBN: 0 7803 7157 7 Material Identity Number: XX-2002-00448
U.S. Copyright Clearance Center Code: 0-7803-7157-7/01/$10.00
Conference Title: Advances in Electronic Materials and Packaging 2001
Conference Sponsor: Korea Sci. & Eng. Found.; Korea Res. Found.; IMAPS-Korea; Samsung Electron.; LG Electron.; Hynix Semicond.; Amkor Technol.; MTS-Korea; Hong Kong Univ. Sci. & Technol.; US Army Res. Office-Far East; Korea-Japan Core Univ. Program
Conference Date: 19-22 Nov. 2001 Conference Location: Jeju Island, South Korea
Language: English
Abstract: Solder bumps on flip **chips** could arrive at the manufacturing floor with prior damage. While bumps with insufficient solder volume may not solder well even if adequately fluxed, the bumps that are flattened during damage are also of concern for fluxing. Good assembly yields will depend on whether these bumps are fluxed adequately and whether the collapse offered by the substrate design is sufficient to bring the damaged **bumps** in **contact** with their target pads. The former depends on the flux application method and the latter depends on the pad design and the solder alloy. When assembled on the same substrates, **lead**-free solder **joints** exhibit less collapse than eutectic tin-**lead** solder. Therefore, a damaged **lead**-free solder **joint** may not solder well even if it is adequately fluxed. The

sensitivity of four flux application methods to bump damage is described in this paper. Solder bumps on flip **chips** were systematically damaged by flattening them to an extent of 40-45 mu m. These damaged **chips** were then assembled using four different fluxing techniques: dip fluxing, stencil printing, flux jetting and no-flow **encapsulation**. Soldering of three alloys, eutectic tin-**lead**, Sn-Ag-Cu (LF2) and Sn-Ag-Cu-In (LF1) was studied. Assembly was followed by X-ray inspection, micro-sectioning and **electrical** testing. As expected, dip fluxing proved to be sensitive to bump damage. Defects were observed with both tin-**lead** and LF2 **chips** with the least flux thickness. Damaged LF1 bumps soldered very well even with a limited amount of flux. Both stencil printing and flux jetting were insensitive to bump damage and resulted in good soldering for all three alloys. The no-flow **encapsulation** process gave good soldering with both tin-**lead** and LF1 **chips** when used with the appropriate reflow profile. Since the reflow **encapsulant** material is designed for use with tin-**lead**, the **encapsulant** gelled before soldering of the LF2 bumps occurred.
Subfile: B


24/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC


7161188 INSPEC Abstract Number: B2002-02-0170J-072
Title: Flip **chip** ball grid array packaging for RFICs
Author(s): Hung, C.P.; Wu, L.; Chiu, C.T.; Hsieh, J.S.; Lee, J.J.
Author Affiliation: Adv. Semicond. Eng. Inc, Kaohsiung, Taiwan
Conference Title: Proceedings 2000 International Symposium on Microelectronics (SPIE Vol.4339) p.28-33
Publisher: IMAPS - Int. Microelectron. & Packaging Soc, Reston, VA, USA
Publication Date: 2000 Country of Publication: USA xx+886 pp.
ISBN: 0 930815 62 9 Material Identity Number: XX-2001-01666
Conference Title: 2000 International Symposium on Microelectronics
Conference Sponsor: SPIE; IMAPS - Int. Microelectron. & Packaging Soc
Conference Date: 18-20 Sept. 2000 Conference Location: Boston, MA, USA
Language: English
Abstract: General advantages of flip-**chip** ball grid array (BGA) are presented with focused topics on electrical characteristics. In this paper high frequency (HF) and radio frequency (RF) are the application fields of the discussed flip **chip IC package** . Comparisons are presented with wire-bond BGA **package** which including the compared **bonding** wire and **bump** performance. Simulation analyzed data for flip-**chip** BGA includes the energy loss, reflection and coupling effects. Time domain comparison between flip-**chip** BGA and wire-bond BGA is illustrated to show the transmitted signal quality. Advantage on saving **electrical connection** space from **die** to substrate is also presented.
Subfile: B


24/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

7049117 INSPEC Abstract Number: B2001-11-0170J-046
Title: Room-temperature interconnection of electroplated Au microbump by means of surface activated bonding method
Author(s): Matsuzawa, Y.; Itoh, T.; Suga, T.
Author Affiliation: Res. Center for Adv. Sci. & Technol., Tokyo Univ., Japan
Conference Title: 2001 Proceedings. 51st Electronic Components and Technology Conference (Cat. No.01CH37220) p.384-7
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA xxxiii+1518 pp.
ISBN: 0 7803 7038 4 Material Identity Number: XX-2001-01138
U.S. Copyright Clearance Center Code: 0 7803 7038 4/2001/$10.00
Conference Title: 51st Electronic Components and Technology Conference 2001. Proceedings
Conference Sponsor: Components, Packaging, & Manuf. Technol. (CPMT) Soc. IEEE; Electron. Components Assemblies & Mater. Assoc. (ECA); Electron. Components Sector of the Electron. Ind. Alliance
Conference Date: 29 May-1 June 2001 Conference Location: Orlando, FL, USA
Language: English
Abstract: Although various bonding methods have been developed for flip-**chip** assembly, most of them cannot be applied to smaller pitch interconnection for the next generation. In the present study, a new bonding method, the surface activated bonding (SAB) is introduced. The feasibility of the SAB for **bump bonding** was investigated by some experiments. The Au electroplated bumps were prepared for experiments. The three different types of material, Au, Cu, and Al were used as contact metals. The reliability of interconnections was tested in temperature storage. As a result, we could achieved the bonding of microbumps with high strength and good **electrical connection**. It was also found that in the **case** of **bump bonding** , SAB can be done under relatively high vacuum pressure condition.
Subfile: B


24/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC


7034218 INSPEC Abstract Number: B2001-10-7230M-024, C2001-10-7410H-035
Title: A mixed-signal sensor interface microinstrument
Author(s): Kraver, K.L.; Guthaus, M.R.; Strong, T.D.; Bird, P.L.; Cha, G.S.; Hold, W.; Brown, R.B.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., Michigan Univ., Ann Arbor, MI, USA
Journal: Sensors and Actuators A (Physical) Conference Title: Sens. Actuators A, Phys. (Switzerland) vol.A91, no.3 p.266-77
Publisher: Elsevier,
Publication Date: 15 July 2001 Country of Publication: Switzerland
CODEN: SAAPEB ISSN: 0924-4247
SICI: 0924-4247(20010715)A91:3L.266:MSSI;1-I
Material Identity Number: N866-2001-010
U.S. Copyright Clearance Center Code: 0924-4247/2001/$20.00
Conference Title: Technical Digest. Solid-State Sensor and Actuator Workshop
Conference Sponsor: Transducers Res. Found

Conference Date: 4-8 June 2000 Conference Location: Hilton Head Island, SC, USA
Language: English
Abstract: A single-**chip** implementation of a microinstrumentation system is presented. The **chip** incorporates voltage, current, and capacitive sensor interfaces: a temperature sensor; a 10-channel, 12-bit analog-to-digital converter; and an and bit microcontroller with a 16-bit hardware multiplier and a 40-bit-accumulator. Serial and parallel interfaces allow digital communication with a host system. Fabricated in a standard 0.35 mu m digital CMOS process, the **die** occupies 3.8 mm*4.1 mm, operates from a nominal supply voltage of 3 V, and draws 16 mA when fully powered (850 mu A standby current). To facilitate testing of the prototype, extra **pads** are **bonded** out to **package** pins. The **chips** are **packaged** in 132-pin ceramic pin-grid-array **packages**.
Subfile: B C


24/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC


7014898 INSPEC Abstract Number: A2001-19-8770J-003, B2001-10-7520E-004
Title: High density interconnects and flexible hybrid assemblies for active biomedical implants
Author(s): Meyer, J.-U.; Stieglitz, T.; Scholz, O.; Haberer, W.; Beutel, H.
Author Affiliation: Fraunhofer-Inst. for Biomed. Eng., St. Ingbert, Germany
Journal: IEEE Transactions on Advanced Packaging vol.24, no.3 p. 366-74
Publisher: IEEE,
Publication Date: Aug. 2001 Country of Publication: USA
CODEN: ITAPFZ ISSN: 1521-3323
SICI: 1521-3323(200108)24:3L.366:HDIF;1-Z
Material Identity Number: H273-2001-003
U.S. Copyright Clearance Center Code: 0 7803 6450 3/2001/$10.00
Language: English
Abstract: Advanced microtechnologies offer new opportunities for the development of active implants that go beyond the design of pacemakers and cochlea implants. Examples of future implants include neural and muscular stimulators, implantable drug delivery systems, intracorporal monitoring devices and body fluid control systems. The active microimplants demand a high degree of device miniaturization without compromising on design flexibility and biocompatibility requirements. With the need for integrating various microcomponents for a complex retina stimulator device, we have developed a novel technique for microassembly and high-density interconnects employing flexible, ultra-thin polymer based substrates. Pads for interconnections, **conductive lines** , and microelectrodes were embedded into the polyimide substrate as thin films. Photolithography and sputtering has been employed to pattern the microstructures. The novel "MicroFlex interconnection (MFI)" technology was developed to achieve **chip** size **package** (CSP) dimensions without the requirement of using bumped flip **chips** (FC). The MFI is based on a rivet like approach that yields an electrical and mechanical **contact** between the **pads** on the flexible polyimide substrate and the bare **chips** or

electronic components. Center to center **bond pad** distances smaller than 100 mu m were accomplished. The ultra thin substrates and the MFI technology was proven to be biocompatible. Electrical and mechanical tests confirmed that interconnects and assembly of bare **chips** are reliable and durable. Based on our experience with the retina stimulator implant, we defined design rules regarding the flexible substrate, the **bond pads**, and the embedded conductive tracks. It is concluded that the MFI opens new venues for a novel generation of active implants with advanced sensing, actuation, and signal processing properties.
Subfile: A B


24/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC


6986215 INSPEC Abstract Number: B2001-09-0170J-002
Title: Electrical and fluidic packaging of surface micromachined electromicrofluidic devices
Author(s): Galambos, P.; Benavides, G.
Author Affiliation: Sandia Nat. Labs., Albuquerque, NM, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.4177 p.200-7
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 2000 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(2000)4177L.200:EFPS;1-X
Material Identity Number: C574-2000-268
U.S. Copyright Clearance Center Code: 0277-786X/2000/$15.00
Conference Title: Microfluidic Devices and Systems III
Conference Sponsor: SPIE
Conference Date: 18-19 Sept. 2000 Conference Location: Santa Clara, CA, USA
Language: English
Abstract: Microfluidic devices have applications in chemical analysis, biomedical devices and ink-jets. An integrated microfluidic system incorporates electrical signals on-**chip**. Such electro-microfluidic devices require fluidic and **electrical connection** to larger **packages** . Therefore electrical and fluidic packaging of electro-microfluidic devices is the key to the development of integrated microfluidic systems. Packaging is more challenging for surface micromachined devices than for larger bulk micromachined devices. However, because surface micromachining allows incorporation of electrical traces during microfluidic channel fabrication, a monolithic device results. A new architecture for packaging surface micromachined electro-microfluidic devices is presented. This architecture relies on two scales of packaging to bring fluid to the device scale (picoliters) from the macroscale (microliters). The architecture emulates and utilizes electronics packaging technology. The larger **package** consists of a circuit board with embedded fluidic channels and standard fluidic connectors. The embedded channels connect to the smaller **package**, an Electro-Microfluidic Dual-Inline-**Package** (EMDIP) that takes fluid to the microfluidic **integrated circuit** (MIC). The fluidic connection is made to the back of the MIC through Bosch etched holes that take fluid to surface micromachined channels on the front of the MIC. **Electrical**

**connection** is made to **bond pads** on the front of the MIC.
Subfile: B


24/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC


6946449 INSPEC Abstract Number: B2001-07-0170J-080
Title: **Wafer** level packaging of a tape flip-**chip chip** scale **packages**
Author(s): Hotchkiss, G.; Amador, G.; Edwards, D.; Hundt, P.; Stark, L.; Stierman, R.; Heinen, G.
Author Affiliation: Texas Instrum. Inc., Dallas, TX, USA
Journal: Microelectronics Reliability vol.41, no.5 p.705-13
Publisher: Elsevier,
Publication Date: May 2001 Country of Publication: UK
CODEN: MCRLAS ISSN: 0026-2714
SICI: 0026-2714(200105)41:5L.705:WLPT;1-O
Material Identity Number: G489-2001-005
U.S. Copyright Clearance Center Code: 0026-2714/2001/$20.00
Language: English
Abstract: The advent of **chip** scale **packages** (CSPs) has led to the development of **wafer** scale assembly (WSA) or **wafer** level packaging (WLP) manufacturing in order to raise assembly efficiencies and lower operating costs. Texas Instruments (TI) has developed a unique WLP process for forming flip-**chip** ball grid array **packages**. The **die** inputs and outputs of the TI CSP are connected through solder bumps to a polyimide film interposer. Solder balls on the other side of the interposer complete the **electrical connection** to the PCB. A **wafer**-sized array of interposers designed to match the **wafer die** pattern is aligned and reflowed to a bumped **wafer**. The TI WLP process is completed by singulating the CSPs from the **wafer** using standard **wafer** saw equipment. Attachment of the interposer to the **die** and application of **die** and board level solder bumps are carried out in **wafer** form using a new bumping technology called Tacky Dots/sup TM/. Tacky Dots uses an array of sticky dots formed in a photosensitive coating laminated to a polyimide film for transferring and attaching solder spheres to semiconductor substrates. A populated film containing one solder sphere per Tacky Dot is positioned over the **wafer** or interposer and lowered until the spheres **contact** the **pads**. A reflow process transfers the spheres from film to **wafer** or interposer and the film is removed once the spheres have frozen. This paper illustrates the process steps and custom equipment developed to form the TI CSP. Strategic use of finite element modeling to optimize the **package** design is outlined. The paper concludes by summarizing **package** level reliability results.
Subfile: B


24/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC


6736775 INSPEC Abstract Number: B2000-12-0170J-007

Title: Flip **chip** **wafer** level packaging of a flexible **chip** scale **package** (CSP)
Author(s): Hotchkiss, G.; Amador, G.; Edwards, D.; Hundt, P.; Stark, L.; Stierman, R.; Heinen, G.
Author Affiliation: Texas Instrum. Inc., Dallas, TX, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3906 p.555-62
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1999 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1999)3906L.555:FCWL;1-J
Material Identity Number: C574-2000-070
Conference Title: 1999 International Symposium on Microelectronics
Conference Sponsor: IMAPS
Conference Date: 26-28 Oct. 1999 Conference Location: Chicago, IL, USA
Language: English
Abstract: The advent of **chip** scale **packages** (CSP) within the semiconductor community has led to the development of **wafer** scale assembly (WSA) or **wafer** level packaging (WLP) manufacturing in order to raise assembly efficiencies and lower operating costs. Texas Instruments (TI) has developed a unique WLP process for forming flip **chip**, ball grid array **packages**. The **die** inputs and outputs of the TI CSP are connected through solder bumps to a polyimide film interposer. Solder balls on the other side of the interposer complete the **electrical** **connection** to a customer's printed circuit board. A **wafer**-sized array of interposers designed to match the pattern of **dies** on a **wafer** is aligned and reflowed to a bumped **wafer**. The TI WLP process is completed by singulating the CSP's from the **wafer** using standard **wafer** saw equipment. Attachment of the interposer to the **die** as well as applying the **die** and board level solder bumps are carried out in wave form using a new bumping technology called Tacky Dots/sup TM/. Tacky Dots uses an array of sticky dots formed in a photosensitive coating laminated to a polymide film for transferring and attaching solder spheres to semiconductor substrates. A populated film containing one solder sphere per tacky dot is positioned over the **wafer** or interposer and lowered until the spheres **contact** the **pads**. A reflow process transfers the spheres from the film to the **wafer** or interposer and the film is removed once the spheres have frozen. This paper illustrates the process steps and custom equipment developed for forming the TI CSP. The strategic use of finite element modeling for optimizing the design of the **package** is outlined. The paper concludes by summarizing the current **package** level reliability results.
Subfile: B


24/3,AB/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC


6735310 INSPEC Abstract Number: B2000-11-0170J-212
Title: Bismuth-filled anisotropically conductive adhesive for flip **chip** bonding
Author(s): Vuorela, M.; Holloway, M.; Fuchs, S.; Stam, F.; Kivilahti, J.
Author Affiliation: Lab. of Electron. Prod. Technol., Helsinki Univ. of

Technol., Espoo, Finland
Conference Title: 4th International Conference on Adhesive Joining and Coating Technology in Electronics Manufacturing. Proceedings. Presented at Adhesives in Electronics 2000 (Cat. No.00EX431) p.147-52
Editor(s): Hyytiainen, M.
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xii+319 pp.
ISBN: 0 7803 6460 0 Material Identity Number: XX-2000-01757
U.S. Copyright Clearance Center Code: 0 7803 6460 0/2000/$10.00
Conference Title: 4th International Conference on Adhesive Joining and Coating Technology in Electronics Manufacturing. Proceedings. Presented at Adhesives in Electronics 2000
Conference Sponsor: NOKIA; IEEE Finland Sect.; Finnish Acad.; Eur. Union; Finnair; CPMT Soc. IEEE; CPMT Finnish Chapter
Conference Date: 18-21 June 2000 Conference Location: Espoo, Finland
Language: English
Abstract: In this communication a new bismuth (Bi)-filled anisotropically conductive adhesive (ACA), which can be used to bond pure tin (Sn) or any Sn-based contact areas, is presented. In this study the adhesive was used to **join** tin-**lead** (SnPb) -bumped test **chips** to SnPb-coated **contact pads** on FR4-substrate. Due to the metallurgical characteristics of the SnPbBi system, the process temperature and bonding pressure remain low. With the help of pure Bi particles, the SnPb bumps are fused with the SnPb-coated **contact pads** above 92 degrees C forming small local solder **joints** , while the adhesive acts as an underfill. The microscopic solder interconnections retain their **electrically** continuity even though the adhesive matrix relaxes in service. Good quality metallurgical interconnections were produced by the bonding procedure with relatively low bonding temperature (160 degrees C) and pressure (24.5 g/bump). No intermetallics are formed in this bonding system. The Bi-filled ACA exhibits good reliability under high temperature and high humidity conditions (85 degrees C/85%RH). Thermal shock test (-40 degrees C/+125 degrees C, total cycle time 1 hour) showed that good reliability can be achieved even though the bonding process is not yet optimized. The failure of the **joints** is due to the formation of small liquid phases in the Bi-rich (over 10 at-%) areas in the solid lentils at the upper thermal shock temperature. This can be avoided by using higher bonding temperature. The discrepancy of reliability results is explained by the fact that the temperature of bonding has not been exactly the same for all the samples bonded.
Subfile: B


24/3,AB/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC


6730478 INSPEC Abstract Number: B2000-11-2550E-114
Title: An investigation on the plasma treatment of **integrated circuit bond pads**
Author(s): Chong, Y.F.; Gopalakrishnan, R.; Tsang, C.F.; Sarker, G.; Lim, S.; Tatti, S.
Author Affiliation: Div. of Mater. Eng., Nanyang Technol. Univ., Singapore
Journal: Microelectronics Reliability vol.40, no.7 p.1199-206
Publisher: Elsevier,

Publication Date: July 2000 Country of Publication: UK
CODEN: MCRLAS ISSN: 0026-2714
SICI: 0026-2714(200007)40:7L.1199:IPTI;1-J
Material Identity Number: G489-2000-006
U.S. Copyright Clearance Center Code: 0026-2714/2000/$20.00
Language: English
Abstract: **Integrated circuit (IC) bond pads** play an important role in the wire bond reliability of **microelectronic** devices. Being the device's only **electrical connection** to the **package** and electronic systems, it is mandatory that the **bond pads** are free of contaminants and possess excellent bonding characteristics. Contaminants such as oxides and organic residues impair the bondability to a considerable extent and are very resistant to conventional wet cleaning methods. In this paper, we report the effects of an Ar-H/sub 2/ plasma treatment on the surface chemistry and morphology of **IC bond pads**. Surface and sub-surface chemical analyses have been conducted using Auger electron spectroscopy (AES), X-ray photoelectron spectroscopy (XPS) and scanning electron microscopy (SEM). Results reveal that the oxygen level of the **bond pad** surface has decreased significantly after the plasma treatment. Although the treatment has successfully removed the surface crystallites on the **bond pads** by prolonged etching; however, the aggressive process has also damaged the passivation layers that surround the pad areas.
Subfile: B


24/3,AB/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC


6703490 INSPEC Abstract Number: B2000-10-0170J-080
Title: **Wafer** level CSP using low cost electroless redistribution layer
Author(s): Teutsch, T.; Oppert, T.; Zakel, E.; Klusmann, E.; Meyer, H.; Schulz, R.; Schulze, J.
Author Affiliation: Pac Tech-Packaging Technol. GmbH, Nauen, Germany
Conference Title: 2000 Proceedings. 50th Electronic Components and Technology Conference (Cat. No.00CH37070) p.107-13
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xxxv+1756 pp.
ISBN: 0 7803 5908 9 Material Identity Number: XX-2000-01366
U.S. Copyright Clearance Center Code: 0 7803 5908 9/2000/$10.00
Conference Title: 2000 Proceedings. 50th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, and Manuf. Technol. Soc. of IEEE; Electronic Ind. Alliance
Conference Date: 21-24 May 2000 Conference Location: Las Vegas, NV, USA
Language: English
Abstract: A driving force to achieve increased speed and performance along with higher I/O count is the Flip **Chip** (FC) Technology which has therefore an high level of importance for a variety of applications. A breakthrough, however, will be the use of flip **chip** due to cost reduction. For this aim it is essential to use low cost bumping techniques. However, to provide FC technologies also for devices with high I/O count

and high pin density applications like Microcontrollers, RAMBUS devices, etc.... it is necessary to redistribute the historically **peripheral bond pads** with ultra fine pad pitch into a **wafer** level CSP. This paper describes a low cost electroless Ni/Au Under Bump Metallization (UBM) and a **wafer** level redistribution process based on electroless copper circuitization. It includes the use of a novel plasma enhanced chemical vapour deposition (PECVD) process to deposit a bifunctional nanolayer acting as an adhesion promotor and as a catalyst for electroless copper deposition. The described techniques are suitable for all **wafer** passivation types, which are used in industry today. The complete redistribution process is based on batch processing and less masking and photoimaging steps. By using the electroless Nickel process and **wafer** level stencil solder printing the process is highly cost efficient and has large volume manufacturing capability. Results and also reliability measurements will be presented. Finally a roadmap regarding the implementation of this process into backend high volume production is shown.

Subfile: B



24/3,AB/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC


6677907 INSPEC Abstract Number: B2000-09-2860C-011

Title: Small-sized dual-band SAW filters using flip-**chip** bonding technology

Author(s): Koshino, M.; Kawase, M.; Kuroda, Y.; Mishima, N.; Takagi, T.; Sakinada, K.; Ebata, Y.; Kimura, S.

Author Affiliation: SAW Eng. Dept., Toshiba Corp., Yokohama, Japan

Conference Title: 1999 IEEE Ultrasonics Symposium. Proceedings. International Symposium (Cat. No.99CH37027) Part vol.1 p.341-6 vol.1

Editor(s): Schneider, S.C.; Levy, M.; McAvoy, B.R.

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 1999 Country of Publication: USA 2 vol. 1760 pp.

ISBN: 0 7803 5722 1 Material Identity Number: XX-2000-01248

U.S. Copyright Clearance Center Code: 0 7803 5722 1/99/$10.00

Conference Title: 1999 IEEE Ultrasonics Symposium. Proceedings. International Symposium

Conference Sponsor: Ultrasonics, Ferroelectr., & Frequency Control Soc

Conference Date: 17-20 Oct. 1999 Conference Location: Caesars Tahoe, NV, USA

Language: English

Abstract: New small-sized dual-band SAW filters have been developed. The filter has the dimension of 3.0*3.0*1.0 mm/sup 3/ and the weight of 30 mg. In order to realize such compact packaging, 62% of surface mount area and 45% of weight of the conventional dual-band SAW filters, we adopt flip-**chip** bonding technology with Au-bumps. The dual-band filter, for Japanese PDC (Personal Digital Cellular) mobile phones, has been realized on a single **chip** . Two cascaded IIDT (Interdigitated Interdigital Transducer) resonator filters with numerous **electrical connections** between **chip** and **package** are easily assembled. To improve mechanical reliability, Al-Cu/Ta-Al/Al-Cu multiple layer film applied to the **bump bonding pads** on the **chip** surface. The developed filter successfully achieves high rejection level of 55 dB at image frequency as well as low insertion loss

of 2.3 dB in the pass-band of around 900 MHz. A two-**chip** dual-band SAW filter with 1.8 GHz and 940 MHz band, with low loss of 2.7 dB, is also developed for DCS (Digital Cellular System) and EGSM (Extended Global System for Mobile communication) dual-band phones.
Subfile: B


24/3,AB/15 (Item 15 from file: 2)
DIALOG(R)File 2:INSPEC


6214936 INSPEC Abstract Number: B1999-05-0170Q-020
Title: Waste treatment for advanced semiconductor packaging operations
Author(s): Brown, P.T.; Raley, B.
Conference Title: Twenty Third IEEE/CPMT International Electronics Manufacturing Technology Symposium (Cat. No.98CH36205) p.286-95
Publisher: IEEE, New York, NY, USA
Publication Date: 1998 Country of Publication: USA xiv+491 pp.
ISBN: 0 7803 4523 1 Material Identity Number: XX-1998-03091
U.S. Copyright Clearance Center Code: 0 7803 4523 1/98/$10.00
Conference Title: Twenty Third IEEE/CPMT International Electronics Manufacturing Technology Symposium. Proceedings 1998 IEMT Symposium
Conference Sponsor: Semicond. Equipment & Mater. Int.; Componemts, Packaging & Manuf. Technol. Soc. IEEE
Conference Date: 19-21 Oct. 1998 Conference Location: Austin, TX, USA
Language: English
Abstract: Due to the maturity of plastic packaging technology in the semiconductor industry, a long history of successful waste treatment and water recycling applications exists. However, new packaging technologies have evolved that do not limit **bond pad** location to the edge of the **die**. These technologies require deposition of a solder **bump** on the **bond pads** for **electrical connection** between **die** and **package** . The solder bump and under bump metallurgy (UBM) can be deposited via electrolytic plating, electroless plating, evaporation, sputtering or other techniques. Many of these metal deposition techniques bring with them new and different metal bearing waste streams that require treatment or disposal. The focus of this paper is on treatment of wastes from electroless plating operations used to deposit the UBM. This process generates several relatively low volume metal bearing concentrated waste streams, and a relatively high volume metal bearing rinse water waste stream. Several waste treatment methods were evaluated to determine the optimum method based on total costs and environmental health and safety (EHS) risks. First, characterization of the wastes and costs for off-site disposal were determined as a worst **case** baseline and fall back position. Second, on-site treatment with sludge generating treatment methods were investigated. Finally, on-site treatment using more elegant nonsludge generating treatment methods were investigated. Although the exact chemistry and process sequence are of course proprietary, the general waste treatment schemes, unit operations and results are presented.
Subfile: B


24/3,AB/16 (Item 16 from file: 2)
DIALOG(R)File 2:INSPEC

6072083 INSPEC Abstract Number: B9812-2570-015
Title: Low-cost flip **chip** technology for organic substrates
Author(s): Baba, S.
Journal: Fujitsu Scientific and Technical Journal vol.34, no.1 p. 78-86
Publisher: Fujitsu,
Publication Date: 1998 Country of Publication: Japan
CODEN: FUSTA4 ISSN: 0016-2523
SICI: 0016-2523(1998)34:1L.78:CFCT;1-6
Material Identity Number: F016-98002
Language: English
Abstract: This paper introduces a flip **chip** technology that is used on various kinds of substrates (glass-epoxy, flexible printed circuit board, and MCM-L/D). In this technology, Au bumps are formed on the **chip** I/O **pads** by wire **bonding** and the **bumps** are pressed onto the substrate pads. The **chip** is bonded and **encapsulated** with a thermosetting adhesive, and conductive paste improves the mechanical and **electrical connection** between the Au bumps and the substrate in order to increase the **connection** reliability. To apply this technology to different types of substrates, we investigated the deformation characteristics of the substrate pad and the adhesive strength and insulation of the adhesive for **encapsulation**. This technology has been applied to some practical products and reduces the mounting areas of LSI to 1/10 or less that of LSI that use the existing SMD **package** approach.
Subfile: B


24/3,AB/17 (Item 17 from file: 2)
DIALOG(R)File 2:INSPEC


5709578 INSPEC Abstract Number: B9711-0170J-070
Title: Board on **chip**-ball grid array (BOC-BGA/sup TM/) **package**. A new design for high frequency application (**package** design and reliability)
Author(s): Chee-Kiang Yew; Pang-Hup Ong; Yong-Khim Swee; Min-Yu Chan; Siu-Waf Low; Toh, J.; Chan, J.; Chew-Weng Leong
Author Affiliation: Dept. of Memory Packaging Dev., Texas Instrum. Singapore, Singapore
Conference Title: 1997 Proceedings. 47th Electronic Components and Technology Conference (Cat. No.97CH36048) p.353-7
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 1294 pp.
ISBN: 0 7803 3857 X Material Identity Number: XX97-01595
U.S. Copyright Clearance Center Code: 0 7803 3857 X/97/$4.00
Conference Title: 1997 Proceedings 47th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, & Manuf. Technol. Soc. IEEE; Electron. Ind. Assoc
Conference Date: 18-21 May 1997 Conference Location: San Jose, CA, USA
Language: English
Abstract: This Board on **chip** -Ball grid array (BOC-BGA/sup TM/) packaging concept has been developed for memory devices to cater for high frequency application. The shorter electric path between **IC**

**chip** and board enable better **electrical** performance. This BOC concept is apply to 1.6 Meg DRAM memory **chip** , with future applications in higher pin counts 64 Meg & 256 Meg DRAM **chips** and other memory products. This paper unveils the BOC-BGA/sup TM/ packaging concept, it uses a board (substrate) material that is mounted above the silicon **chip** as in the **case** of **Lead** On **Chip** (LOG) technology. Beside using in DRAM packaging, the concept is applicable to any silicon **chips** such as VRAM, LOGIC, SRAM, EPROM and other **integrated circuit chip** which required array form of interconnect. The sawing, mounting, and bonding processes can be carried out on the existing assembly and test equipment. The interconnect from the **bond pads** to the solder balls is achieved through copper traces and via holes within the substrate. New processes such as underfill, liquid compound **encapsulation** , ball mounting and reflow need to be implemented. This paper outlines the design and reliability considerations for 16 Meg BOC-BGA **package** . The design-in computer simulation is carried out at the beginning of packaging design, software are used to access and select the optimum design from Thermal, **Electrical** and Thermal Stress requirements. This final design will encompass good heat dissipation, low **electrical** inductance, low stress and warpage characteristics. In **package** reliability test, the 16 Meg BOC-BGA **package** pass level 2 & 3 Popcorn Test, Pressure Cooker Test and completed 200 and 500 Temperature Cycling without any external **package** crack and delamination. Board level solder **joint** reliability is currently on-going.

Subfile: B



24/3,AB/18 (Item 18 from file: 2)
DIALOG(R)File 2:INSPEC


5709576 INSPEC Abstract Number: B9711-0170J-068

Title: A thermally enhanced plastic **package** with indented leadframe

Author(s): Lee, C.C.; Chien, D.H.

Author Affiliation: Dept. of Electr. & Comput. Eng., California Univ., Irvine, CA, USA

Conference Title: 1997 Proceedings. 47th Electronic Components and Technology Conference (Cat. No.97CH36048) p.338-42

Publisher: IEEE, New York, NY, USA

Publication Date: 1997 Country of Publication: USA 1294 pp.

ISBN: 0 7803 3857 X Material Identity Number: XX97-01595

U.S. Copyright Clearance Center Code: 0 7803 3857 X/97/$4.00

Conference Title: 1997 Proceedings 47th Electronic Components and Technology Conference

Conference Sponsor: Components, Packaging, & Manuf. Technol. Soc. IEEE; Electron. Ind. Assoc

Conference Date: 18-21 May 1997 Conference Location: San Jose, CA, USA

Language: English

Abstract: A new plastic **package** with indented leadframe is proposed. The unique feature of the new design is that the **die**-pad region is indented to expose its bottom surface to the **package** exterior. The potential advantages of this **package** design are: 1. the exposed **die**-pad surface can be soldered to a thermal via in the PCB, providing the shortest possible heat path from the **die** to the board for the best possible thermal performance. 2. the additional solder

**joint** greatly enhances the mechanical strength and reliability of the PCB assembly. 3. since the **die** top surface is almost in plane with the **bonding pads** on the leadframe, the wire bonding process is easier and the wire can be shortened to reduce inductance. 4. being soldered to the PCB, the **die** -pad region can serve as the best possible **electrical** ground. In assembly, the exposed **die**-pad is mounted in the same soldering operation as the **leads**. Thus, the cost of the above performance improvements is only a few extra stamping steps for the **die** -pad indention. Comparing to other thermal enhancement features, the present **package** design can be implemented at lower cost. Finite element analyses of the new **package** of the same footprint as a 16-**lead** SOIC double batwing **package** shows that it compares favorably with the heat slug enhanced SOIC **package** in terms of thermal performance.

Subfile: B



24/3,AB/19 (Item 19 from file: 2)
DIALOG(R)File 2:INSPEC


5553923 INSPEC Abstract Number: B9705-0170N-017

Title: The role of RIE in microchip **bond pad** corrosion

Author(s): Brownson, R.; Butler, K.; Cadena, S.; Detar, M.; Johnson, I.; McCoulloch, L.; McCoulloch, J.; Mishra, B.; Healey, J.; Honcik, K.; Phan, T.; Sterif, T.; Stevens, H.; Tovar, A.

Author Affiliation: Semicond. Products Sector, Motorola Inc., Austin, TX, USA

Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.2874 p.95-102

Publisher: SPIE-Int. Soc. Opt. Eng,

Publication Date: 1996 Country of Publication: USA

CODEN: PSISDG ISSN: 0277-786X

SICI: 0277-786X(1996)2874L.95:RMBC;1-B

Material Identity Number: C574-96226

U.S. Copyright Clearance Center Code: 0 8194 2272 X/96/$6.00

Conference Title: Microelectronic Manufacturing Yield, Reliability, and Failure Analysis II

Conference Sponsor: SPIE

Conference Date: 16-17 Oct. 1996 Conference Location: Austin, TX, USA

Language: English

Abstract: The discoloration of microchip **bond pads** due to the corrosive effects of the chemistries to which they are exposed poses a special problem for subsequent wire bonding operations. Such corrosion constitutes not only a cosmetic defect, but also interferes with the adhesion of the gold ball bonds to the **bonding pads** and compromises **electrical connections** to the device. These defects pose a serious reliability problem, and precautions must be taken in the manufacture of **microelectronic** devices to ensure that **bond pad** corrosion does not occur. This paper describes the phenomenon of **bond pad** staining/corrosion and the factors which influence its occurrence. A series of experiments were conducted to isolate and understand the corrosion mechanism, and the results of these experiments are presented. Finally, two different process modifications are presented which eliminate the occurrence of **bond pad** corrosion: a double

sintering process, and the elimination of RF sputter etch prior to TiN ARC deposition on the top metal layer.
Subfile: B


24/3,AB/20 (Item 20 from file: 2)
DIALOG(R)File 2:INSPEC


5362651 INSPEC Abstract Number: B9610-2240-006
Title: Solderless flip **chip** bump process technology
Author(s): Estes, R.S.
Author Affiliation: Epoxy Technol. Inc., Billerica, MA, USA
Conference Title: SMI Surface Mount International. Advanced Electronics Manufactuting Technologies. Proceedings of the Technical Program p. 156-70
Publisher: SMTA, Edina, MN, USA
Publication Date: 1995 Country of Publication: USA 1082 pp.
Material Identity Number: XX96-01150
Conference Title: Proceedings of Surface Mount International Conference
Conference Date: 29-31 Aug. 1995 Conference Location: San Jose, CA, USA
Language: English
Abstract: Currently, flip **chip** interconnect technology is rapidly gaining momentum as the **microelectronics** industry strives to meet the challenges of increasing circuit speed, density and function without sacrificing the size and weight of the module assemblies. Increasing the number of I/O connections on a semiconductor device to the levels needed for the next generation of electronic packaging requires significant changes in circuit design, **bond pad** layout and the interconnection method used to make the **electrical connections**. This paper describes the work being conducted on solderless flip **chip** bump process technology as a method for making **electrical connections** between semiconductor **chips** and circuit substrates. Comparisons are made to "solder bump" flip **chip** processes, and reliability and applications data are presented on circuits fabricated with this process. As a final topic, data on flip **chip** underfill and future applications is presented.
Subfile: B


24/3,AB/21 (Item 21 from file: 2)
DIALOG(R)File 2:INSPEC


5337355 INSPEC Abstract Number: B9609-0170J-048
Title: Flip **chip** interconnect: a versatile known good **die** technology
Author(s): Chrusciel, R.W.; Delivorias, P.; Rispoli, K.
Author Affiliation: ETEC Inc., Peabody, MA, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.2649 p.384-9
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1995 Country of Publication: USA

CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1995)2649L.384:FCIV;1-N
Material Identity Number: C574-96033
Conference Title: 1995 International Symposium on Microelectronics
Conference Sponsor: Microelectron. Soc
Conference Date: 24-26 Oct. 1995 Conference Location: Los Angeles, CA, USA
Language: English
Abstract: Using advanced packaging process technologies, bare **die** can be **connected** to a temporary **package**, sealed and **electrically** tested to specification requirements, without compromising the quality or reliability of the **die**. This paper presents a temporary flip **chip** interconnect technology that is applied through the use of a multi-stage robotic station placing the flipped **die** onto a test substrate, prepared with dispensed or screened thermoplastic bumps. These **electrically** conductive bumps are formulated to penetrate the native aluminum oxide of the inverted **die** 's **bond pads** at elevated temperature under Z-axis pressure. This flip **chip** interconnect sequence requires no topographical alterations to the **die** . Thin or thick films as well as laminated board technologies can be used in fabrication of the test carrier. The selection of a substrate reflects cost and/or pad fan-out line density requirements. The original quality and reliability of the tested **die** are retained since the thermoplastic bump material leaves no residue on the **bond pads** of the tested **die**. This process eliminates concerns regarding **connector** /contact quality on subsequent wire bonding for final **package** assembly.
Subfile: B


24/3,AB/22 (Item 22 from file: 2)
DIALOG(R)File 2:INSPEC


5309653 INSPEC Abstract Number: B9608-2575-030
Title: Anodically bonded silicon membranes for sealed and flush mounted microsensors
Author(s): Trautweiler, S.F.; Paul, O.; Stahl, J.; Baltes, H.
Author Affiliation: Phys. Electron. Lab., Eidgenossische Tech. Hochschule, Zurich, Switzerland
Conference Title: Proceedings. IEEE, The Ninth Annual International Workshop on Micro Electro Mechanical Systems. An Investigation of Micro Structures, Sensors, Actuators, Machines and Systems (Cat. No.96CH35856) p.61-6
Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA xxiv+530 pp.
ISBN: 0 7803 2985 6 Material Identity Number: XX96-00338
U.S. Copyright Clearance Center Code: 0 7803 2985 6/96/$5.00
Conference Title: Proceedings of Ninth International Workshop on Micro Electromechanical Systems
Conference Sponsor: IEEE Robotics & Autom. Soc
Conference Date: 11-15 Feb. 1996 Conference Location: San Diego, CA, USA
Language: English
Abstract: This paper reports a novel fabrication process which improves the thermal isolation of silicon membrane structures and allows the

resulting devices to be flush mounted in a wall keeping the electronically active side of the membrane **protected** from the medium to be measured. Silicon **wafers** are bonded anodically with their processed front to Pyrex glass substrates. After the silicon is etched down to about 15 mu m the bonded **wafers** are diced. The separated devices are glued onto ceramic substrates and **electrically connected** by wire **bonds**. The **bonding pads** of the device are located on the membrane and the wires are applied through holes in the glass substrate. Only the rear of the membrane is exposed to the medium while the electronically active side and the **electrical connections** are sealed. Important thermal and mechanical properties are derived from finite element models and measurements. Finally, we demonstrate this new approach by the fabrication and characterization of membrane-based thermal flow sensors.

Subfile: B



24/3,AB/23 (Item 23 from file: 2)
DIALOG(R)File 2:INSPEC


5237138 INSPEC Abstract Number: B9605-0170J-145

Title: A comparison of flip **chip** technology with **chip** size **packages**

Author(s): Simon, J.; Topper, M.; Reichl, H.; Chmiel, G.

Author Affiliation: Forschungsschwerpunkt Technol. der Mikroperipherik, Tech. Univ. Berlin, Germany

Conference Title: Proceedings of the 1995 International Electronics Packaging Conference p.665-74

Publisher: Int. Electron. Packaging Soc, Wheaton, IL, USA

Publication Date: 1995 Country of Publication: USA 826 pp.

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Conference Title: Proceedings of 1995 International Electronics Packaging Conference

Conference Sponsor: Int. Electron. Packaging Soc

Conference Date: 24-27 Sept. 1995 Conference Location: San Diego, CA, USA

Language: English

Abstract: The advantages of flip **chip** technology concerning electrical performance and small mounting area are well known. Unfortunately, most of the available **dice** are not designed for flip **chip** applications with the **bond pad** area arrangement. At least for the immediate future, it must be assumed that the majority of **integrated circuits** will be used in **packages** and therefore will have **peripheral** bondpads. If **die** size is determined by the **peripheral** bondpads, size shrinkage requires pitch reduction. A reduced pitch may limit use as a flip **chip**. Hence **chip** size **packages** (CSP) offer a solution to this problem. The CSP allows matching of the fine **peripheral** pitch to an area arrangement with increased pitch. The additional packaging level of the CSP gives several advantages: the rewiring allows a standardization. The standardization is beneficial for standardized test equipment, e.g. for burn-in. The CSP is thus be an alternative to the KGD as the CSP has approximately the same dimensions as the bare **die**. To demonstrate the benefits of the CSP a FC-BGA was developed on **wafer** level. The FC-BGA uses multilayer and bumping technologies for rewiring the **peripheral**

bondpads to an area array. A **die** with 328 I/Os and a **peripheral** pitch of 100 mu m was used as a test sample. Rewiring resulted in a pitch of 350 mu m, which is suitable for PCBs.
Subfile: B


24/3,AB/24 (Item 24 from file: 2)
DIALOG(R)File 2:INSPEC


5186633 INSPEC Abstract Number: B9603-2860C-012
Title: Miniaturized SAW filters using a flip-**chip** technique
Author(s): Yatsuda, H.; Horishima, T.; Eimura, T.; Ooiwa, T.
Author Affiliation: Japan Radio Co. Ltd., Saitama, Japan
Journal: IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control vol.43, no.1 p.125-30
Publisher: IEEE,
Publication Date: Jan. 1996 Country of Publication: USA
CODEN: ITUCER ISSN: 0885-3010
SICI: 0885-3010(199601)43:1L.125:MFUF;1-K
Material Identity Number: J776-96001
U.S. Copyright Clearance Center Code: 0885-3010/96/$05.00
Language: English
Abstract: This paper describes a miniature surface acoustic wave (SAW) filter, 3.2*2.5*0.9 mm/sup 3/, which is applicable for radio frequency (RF) stage filters in mobile phones. The SAW filter is reduced in size by using a flip-**chip** assembly technique. The technique uses gold bumps on the SAW **chip** and gold-gold thermosonic face-down **bonding**. The gold **bumps** are formed onto the **wafer** by a conventional wire bonding machine using gold wire. The thermosonic face-down bonding enables the **connection** of gold bumps on the SAW **chip**, with gold metallized pads, on a ceramic **package** at a temperature below 200 degrees C. This bonding ensures that the SAW **chip** is fixed mechanically, and **connected electrically**, with the **package** . Frequency responses of a 950-MHz flip-**chip** SAW filter are compared with responses of a SAW filter with a conventional **package**. The results of reliability tests for flip-**chip** SAW filters are shown.
Subfile: B


24/3,AB/25 (Item 25 from file: 2)
DIALOG(R)File 2:INSPEC


4750920 INSPEC Abstract Number: B9410-0170L-026, C9410-7410D-056
Title: Computer vision system for the measurement of **IC** wire-bond height
Author(s): Zhang, W.; Koh, L.M.; Wong, E.M.C.
Author Affiliation: Sch. of Electr. & Electron. Eng., Nanyang Technol. Univ., Singapore
Part vol.2 p.948-51 vol.2
Editor(s): Yuan Baozong
Publisher: IEEE, New York, NY, USA
Publication Date: 1993 Country of Publication: USA 5 vol. (xxvi+1206+xvii+676+xv+580+xvii+619) pp.

ISBN: 0 7803 1233 3
Conference Title: Proceedings of TENCON '93. IEEE Region 10 International Conference on Computers, Communications and Automation
Conference Date: 19-21 Oct. 1993 Conference Location: Beijing, China
Language: English
Abstract: In the production of **integrated circuits** (**ICs**), the wire-bond operation constructs an **electrical connection** between the **bond pads** and the **package leads** using fine gold wire with diameter ranging from 25 mu m to 65 mu m. Good quality control of the bonding operation requires the bonded ball diameter and height on the aluminum pad of the silicon **chip** to be within a certain specified tolerance. This paper describes a low-cost and high-speed visual inspection system for the automatic measurement of the wire-bond ball height using a structured lighting technique. This method is superior to other possible techniques reported so far, because of its potential in online implementation. The system can measure the wire-bond height to an accuracy of +or-3 mu m. Higher accuracy can be achieved with a higher resolution camera and video frame grabber.
Subfile: B C

24/3,AB/26 (Item 26 from file: 2)
DIALOG(R)File 2:INSPEC


4595452 INSPEC Abstract Number: B9403-0170J-072
Title: Four layer metal, flip **chip**, submicron ASIC product designed for advanced multichip module
Author(s): Grula, J.; Blood, W.
Author Affiliation: Motorola Inc., Chandler, AZ, USA
Conference Title: Proceedings of Fifth Annual IEEE International ASIC Conference and Exhibit (Cat. No.92TH0475-4) p.238-41
Editor(s): Tsai, Y.T.; d'Luna, L.J.; Lee, P.P.K.
Publisher: IEEE, New York, NY, USA
Publication Date: 1992 Country of Publication: USA xxii+583 pp.
ISBN: 0 7803 0768 2
U.S. Copyright Clearance Center Code: 0 7803 0768 2/92/$03.00
Conference Sponsor: IEEE; Eastman Kodak; PR Commun
Conference Date: 21-25 Sept. 1992 Conference Location: Rochester, NY, USA
Language: English
Abstract: The use of an additional metal layer on a large CMOS ASIC part provides a practical method for converting an existing **chip** design with wirebond or tape automated **bonding** (TAB) **peripheral pads** to an array of flip **chip** solder bumps across the **chip** surface. While there are advantages to single **chip packages** with flip **chip** interconnect, multichip modules are required to take full advantage of flip **chip** packing density and performance gains. Compared with single **chip packages** on a printed circuit board, flip **chip** multichip modules offer about a 10* surface area reduction. Propagation delays in signal interconnect lines are about three times faster for the module than single **chip packages** on a printed circuit board.
Subfile: B

24/3,AB/27 (Item 27 from file: 2)

DIALOG(R)File 2:INSPEC


4592326 INSPEC Abstract Number: B9403-0170J-058
Title: High **pad** plated solder **contacts** for surface mounted devices
Journal: Elektronik Praxis vol.28, no.21 p.122-4
Publication Date: 4 Nov. 1993 Country of Publication: West Germany
CODEN: EKPXAM ISSN: 0341-5783
Language: German
Abstract: Describes plated tin-**lead** solder pads on nickel tracks stated to achieve high precision and therefore reduced solder shorts. This method is reported to require no solder paste application and it is claimed that it can be used for **connection** pitches down to 0.5 millimetres. Applications include mounting of **integrated circuit packages** with up to 300 connections.
Subfile: B

24/3,AB/28 (Item 28 from file: 2)
DIALOG(R)File 2:INSPEC


4523499 INSPEC Abstract Number: B9312-0100-052
Title: Electronic troubleshooting
Author(s): Matsuda, D.
Publisher: Prentice Hall, Englewood Cliffs, NJ, USA
Publication Date: 1992 Country of Publication: USA vii+472 pp.
ISBN: 0 13 248055 7
Language: English
Abstract: This book contains sixteen chapters covering the following topics: the approach to troubleshooting; DC voltage checks for locating defective parts; checking **conductors**, **connectors**, and power input circuits; troubleshooting branching paths; in-circuit checks; basic and regulated power supplies; checking signal circuits; troubleshooting basic transistor circuits; high-frequency, wideband and related circuits; monochrome and colour display tube circuits; linear **IC chips**; checking voltages and resistances in digital circuits.
Subfile: B

24/3,AB/29 (Item 29 from file: 2)
DIALOG(R)File 2:INSPEC


04396772 INSPEC Abstract Number: A9311-4282-019, B9306-7230C-014
Title: A method for determining the yield of indium **bump contacts** for integration in hybrid focal plane arrays at room temperature
Author(s): Bhan, R.K.; Lomash, S.K.; Chhabra, K.C.
Author Affiliation: Solid State Phys. Lab., Delhi, India
Journal: Infrared Physics vol.34, no.1 p.43-8
Publication Date: Feb. 1993 Country of Publication: UK
CODEN: INFPAD ISSN: 0020-0891
U.S. Copyright Clearance Center Code: 0020-0891/93/$6.00+0.00
Language: English
Abstract: A simple electrical method for determining the yield of indium

bump integration between the infrared photosensing **chip** and the silicon readout **chip** in hybrid focal plane arrays (FPAs) is proposed. In the authors **case**, the IR photosensing **chip** consists of a 16*16 HgCdTe (MCT) photovoltaic (PV) array and the readout **chip** is a 16*16 silicon-CCD multiplexer (MUX). However, the method can be used for even larger array sizes. The method allows one to determine the yield of integration at room temperature. In addition, it does not necessitate the vacuum sealing of hybrid FPA in the dewar and subsequent testing at 77 K for determining this yield. The proposed method essentially verifies the **electrical connectivity** between the MCT PV diodes and their corresponding input diffusions in the CCD MUX on pixel-to-pixel basis. A simple examination of the readout of the whole array on the oscilloscope at room temperature, initiated at the detector and through CCD MUX is used for determining exactly how many MCT PV diodes have been joined successfully to their corresponding CCD MUX pixels after indium bump integration.
Subfile: A B

24/3,AB/30 (Item 30 from file: 2)
DIALOG(R)File 2:INSPEC


04016169 INSPEC Abstract Number: B91080606
Title: Development of continuous compression tool for full tension **conductor connector**
Author(s): Miyabe, T.; Hamada, Y.; Sugo, Y.; Yoshitomi, K.
Author Affiliation: Fujikura Ltd., Tokyo, Japan
Journal: Fujikura Technical Review no.20 p.51-7
Publication Date: Jan. 1991 Country of Publication: Japan
CODEN: FKDGAO ISSN: 0429-8357
Language: English
Abstract: Overhead distribution wires, especially aluminum distribution wires, have been joined by using compression typed full tension **conductor connectors**. These connectors have been compressed by a compression tool of a manual type or engine driven type. The capacity of these compression tools are limited from workabilities such as weight, handling property and dimensions. The 12 tons class compression tools have been mainly used. The compression **dies** also limit the compression width up to 20 mm due to the capacity of the compression tool. Accordingly, a long connector such as a tension connector for ACSR (aluminum conductor steel reinforced) 120 mm/sup 2/ conductor has to be compressed 30 times. This is very heavy work for linemen. Fujikura have developed a rotary **die** type continuous compression tool to solve these problems. The authors describe the concept of the design of the tool and electrical properties of the full tension **conductor connectors** which are compressed by this tool.
Subfile: B

24/3,AB/31 (Item 31 from file: 2)
DIALOG(R)File 2:INSPEC


03581218 INSPEC Abstract Number: B90021360
Title: High-density multichip module by **chip**-on-**wafer** technology
Author(s): Kimijima, S.; Miyagi, T.; Sudo, T.; Shimada, O.

Author Affiliation: R&D Center, Toshiba Corp., Kawasaki, Japan
Journal: Hybrid Circuits no.21 p.33-5
Publication Date: Jan. 1990 Country of Publication: UK
CODEN: HYCRD5 ISSN: 0265-3028
Language: English
Abstract: A high-density module for image processing was developed by **chip**-on-**wafer** technology. A silicon **wafer** was used as the substrate and the LSI **chips** were flip-**chip** bonded to the silicon **wafer** by bumps in **chip**-on-**wafer** technology. A primary benefit of using a silicon **wafer** is the small induced thermal stress which affects the bumps. The module contained a digital signal processor, SRAMs and other **peripheral** LSIs. A total of sixteen **chips** were bonded on the **wafer**. The LSIs were connected to each other by copper/polyimide multilayer interconnections consisting of eight copper conductive layers and polyimide dielectric layers. The characteristic impedance for the signal lines was controlled to 50 ohms. The LSIs were connected to the **wafer** electrically and mechanically by solder bumps, which were formed on the LSI **bonding pads**. A 188 pin AlN ceramic **package** was used for the module in order to obtain high heat radiation and high reliability. The occupied area for the module was reduced to 20%, compared with the size for conventionally assembled DIPs on a PC board.
Subfile: B

24/3,AB/32 (Item 32 from file: 2)
DIALOG(R)File 2:INSPEC


02204829 INSPEC Abstract Number: B84014034
Title: Large scale integration (LSI) **chip** carriers
Author(s): Crisanti, J.P.; Desai, B.C.
Author Affiliation: E.I. du Pont de Nemours & Co. Inc., Camp Hill, PA, USA
Journal: International Journal for Hybrid Microelectronics vol.6, no.1 p.34-9
Publication Date: Oct. 1983 Country of Publication: USA
CODEN: IMICDJ ISSN: 0277-8270
Conference Title: 1983 International Microelectronics Symposium
Conference Date: 31 Oct.-2 Nov. 1983 Conference Location: Philadelphia, PA, USA
Language: English
Abstract: The development of the **Joint** Electron Devices Engineering Council (JEDEC) ceramic **chip** carriers has created a demand for new high density printed wiring board interconnections. The technical challenges of this packaging concept include thermal management, high speed **electrical** performance and reliability of the interconnect over a wide range of environmental conditions. In addition, provisions must be made to handle **contact pad** centerline spacings of 50, 40, 25, and 20 mils. The leaded **chip** carriers described meet these challenges through the use of clip type terminals and advanced processing techniques. These clips allow the user to terminate high **lead** count ceramic **packages** to printed wiring boards by solving the problems of thermal mismatch, high speed **electrical** performance and termination cost. The authors describe the product application, the test methods used, and the results obtained during the evaluation of this termination approach.
Subfile: B

24/3,AB/33 (Item 33 from file: 2)
DIALOG(R)File 2:INSPEC


01167623 INSPEC Abstract Number: B78014638
Title: Method of separating **wafers** having **contact-pad** devices
Author(s): Felker, D.E.
Author Affiliation: Weston Electric, Allentown, PA, USA
Journal: Technical Digest no.47 p.7
Publication Date: July 1977 Country of Publication: USA
CODEN: TCHDAV ISSN: 0497-0411
Language: English
Abstract: Describes a solution to the problem of separating a **wafer** into individual **chips** when **contact pads** rather than beam leads are used for the **electrical connections**. The procedure greatly reduces the volume of the material which must be removed. The **chip** is much thicker and therefore stronger because the **wafer** does not have to be reduced to approximately 2 mils thick before etching. Since the **wafer** will not have to be thinned, the mounting of the **wafer** on the support disc is no longer critical. When compared to sawing through the entire **wafer**, the etch-saw technique is faster. It eliminates the need for a **protective**, sacrificial film between the **wafer** and the support disc to prevent the saw from cutting the support disc while assuring full separation of **chips**.
Subfile: B

24/3,AB/34 (Item 34 from file: 2)
DIALOG(R)File 2:INSPEC


00981484 INSPEC Abstract Number: B76046476, C76028301
Title: A high-density, read/write, nonvolatile charge-addressed memory
Author(s): Fagan, J.L.; White, M.H.; Lampe, D.L.
Author Affiliation: Westinghouse Electric Corp., Baltimore, MD, USA
Conference Title: 1976 IEEE International Solid-State Circuits Conference. (Digest of technical papers) p.184-5
Editor(s): Winner, L.
Publisher: IEEE, New York, NY, USA
Publication Date: 1976 Country of Publication: USA 249 pp.
Conference Sponsor: IEEE
Conference Date: 18-20 Feb. 1976 Conference Location: Philadelphia, PA, USA
Language: English
Abstract: Describes a memory cell and **peripheral** address-detection circuit combination to achieve array densities of 0.5 mil/sup 2//bit with 10 mu m aluminum lines and spacings, combined with 6 mu m polysilicon lines and 10 mu m polysilicon spacings. The cell and **peripheral** address circuitry are combined to form a 16K-bit memory **chip** in an area of 100 mils*200 mils, exclusive of **bonding pads** and scribe lanes. The memory **chip** is TTL compatible and fabricated with 6 photolithographic steps, exclusive of **bonding pad protection**.
Subfile: B C

24/3,AB/35 (Item 35 from file: 2)
DIALOG(R)File 2:INSPEC


00394528 INSPEC Abstract Number: B72021284
Title: An instrument for measuring electrical conductivity and the rate of its increase
Author(s): Patocka, Z.; Netuka, J.
Journal: Sdelovaci Technika vol.20, no.2 p.48-50
Publication Date: 1972 Country of Publication: Czechoslovakia
CODEN: SDTEAM ISSN: 0036-9942
Language: Czech
Abstract: The principle, design and operational characteristics of this instrument are described. For the measurement of the conductivity, a circuit employing an operational amplifier to whose parallel network is connected the measured conductivity, is used. For the measurement of the rate of increase of the conductivity, a derivative circuit is connected into the measuring circuit. The method of suppressing the influence of the **conducting connectors** is discussed. The application of this instrument in the manufacture of thin conducting layers is considered.
Subfile: B

24/3,AB/36 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS


0503382 NTIS Accession Number: AD-A010 782/1/XAB
Hardened Hybrid Semiconductor **Packages**. Task II
(Final rept. 1 Jan-31 Jan 75)
Lindberg, F. A.
Westinghouse Defense and Electronic Systems Center Baltimore Md Systems Development Div
Corp. Source Codes: 405897
Sponsor: Harry Diamond Labs., Adelphi, Md.
Report No.: 75-0516; HDL-CR-75-216-1
May 75 27p
Journal Announcement: GRAI7516
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A03/MF A01
The work was performed to develop a radiation hardened packaging technique for packaging a whole round semiconductor **wafer**. The metal which connected the **wafer bonding pads** to the **package** output pins was aluminum which was vapor deposited through a mask on the inside surface of the **package**. One end of each **conductor line** was lifted off the **package** surface to form a beam lead. These beam leads were then ultrasonically bonded to the **wafer bonding pads**.

24/3,AB/37 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05246120
E.I. No: EIP99034595375
Title: Introduction to **electrically** conductive adhesives
Author: Li, Li; Morris, J.E.
Corporate Source: Motorola Semiconductor Products Sector, Tempe, AZ, USA
Source: International Journal of Microelectronic Packaging Materials and Technologies v 1 n 3 1998. p 159-175
Publication Year: 1998
CODEN: IJMTF3 ISSN: 1023-6228
Language: English
Abstract: **Electrically** conductive adhesives (ECA) can be used to provide both mechanical bond and **electrical** interconnection between a device **lead** or **chip** carrier and a circuit board **contact pad**. This dual functionality is achieved by composite materials composed of metallic particles dispersed in an adhesive matrix. There are several types of conductive adhesives divided by their morphology, metal filler percentage, and processing requirements. These types are: isotropic conductive adhesives (ICA); anisotropic conductive adhesives (ACA); anisotropic conductive adhesive films (ACAF); heat seal **connectors** (HSC); and non-conductive adhesives (NCA). 117 Refs.

24/3,AB/38 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)


05171225
E.I. No: EIP98124490808
Title: Optimization study of thermal path from plastic **packages** to board
Author: Lee, Chin C.; Chien, David H.; Tsai, Chen S.
Corporate Source: Univ of California, Irvine, CA, USA
Source: International Journal of Microcircuits and Electronic Packaging v 21 n 1 First Quarte 1998. p 93-99
Publication Year: 1998
CODEN: IMICDJ ISSN: 1063-1674
Language: English
Abstract: A study is carried out to optimize the thermal path from plastic **packages** to Printed Circuit Board (PCB). Various thermal enhancement features are investigated in this work to improve the thermal path. This effort results in a new leadframe design of which the **die** -pad region is indented to expose its bottom surface to the **package** exterior. The potential advantages of this indented leadframe **package** are: 1) the exposed **die**-pad surface can be soldered to a thermal via in the printed circuit board, thus providing the shortest possible thermal path from the **die** to the board, 2) the additional solder **joint** greatly enhances the mechanical strength and reliability of the PCB assembly, 3) since the **die** surface is almost in plane with **bonding pads** on the leadframe, wire bonding process is easier and the wires can be shortened to reduce inductance, and 4) being soldered to the PCB, the **die**-pad region also serves as the best possible **electrical** ground. Since the exposed **die**-pad is mounted in the same soldering operation as the **leads** during assembly, the extra cost of the above improvements is due to a few extra stamping steps for the **die** pad indentation. Thus, this new **package** design can be

implemented at low cost. Finite Element analysis has been performed on 16-**lead** Small Outline **Integrated Circuit** (SOIC) double batwing **package** mounted on a PCB. Several thermal enhancement features as well as the new **package** are modeled in the analysis. The results show that the indented leadframe **package** compares favorably with the heat slug enhanced SOIC **package** in thermal performance. (Author abstract) 15 Refs.

24/3,AB/39 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)


04978012
E.I. No: EIP98034132993
Title: FIB techniques to debug flip-**chip integrated circuits**
Author: Livengood, Richard H.; Rao, Valluri R.
Corporate Source: Intel Corp, Santa Clara, CA, USA
Source: Semiconductor International v 21 n 3 Mar 1998. p 111-112, 114, 116
Publication Year: 1998
CODEN: SITLDD ISSN: 0163-3767
Language: English
Abstract: An alternative to conventional wirebond packaging for **integrated circuit** manufacture is flip-**chip** packaging, also known as C4 (controlled-collapse **chip connection**). C4 packaging allows direct **electrical connection** between the **chip** and the **package** through solder **bumps** that **connect bonding pads** on the **chip** to corresponding pads on the **package**. Unlike wirebond technology which only allows **peripheral bonding**, C4 **bumps** can be placed anywhere on the **die**. This **leads** to very low inductance power distribution to the **chip**, which is one of the major advantages of C4. 4 Refs.

24/3,AB/40 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)


04065084
E.I. No: EIP95022566532
Title: TBGA **package** technology
Author: Andros, Frank E.; Hammer, Richard B.
Corporate Source: IBM Corp, Endicott, NY, USA
Source: IEEE Transactions on Components, Packaging, and Manufacturing Technology Part B: Advanced Packaging v 17 n 4 Nov 1994. p 564-568
Publication Year: 1994
CODEN: IMTBE4 ISSN: 1070-9894
Language: English
Abstract: TBGA or Tape Ball Grid Array is a ball grid array **package** which utilizes solder bumps to connect the TAB tape to the printed circuit card or board. The array of outer **lead** bond (OLB) joints is typically on a 50 mil grid. This technology differs from conventional TAB **peripheral** OLB in that the **package** can be 'picked and placed' using conventional card assembly equipment and processes at very high assembly yields. If thermal enhancement is required, a heatsink can be

attached to the **die**. The technology can be applied to both single and double level metal tape; and can utilize various inner **lead** bonding (ILB) techniques, i.e., **peripheral** thermocompression, thermosonic, or wirebonding, and area array solder reflow. This paper describes the **package** technology, applications, and attributes. (Author abstract) 6 Refs.

24/3,AB/41 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)


03724693
E.I. No: EIP93101093817
Title: 820 pin PGA for ultra large-scale BiCMOS devices
Author: Hiruta, Y.; Hirano, N.; Itoh, K.; Kato, K.; Yamaji, Y.; Motoyama, Y.; Ohno, J.; Homma, R.; Kojima, S.; Sudo, T.
Corporate Source: Toshiba Corp, Kawasaki, Jpn
Conference Title: 1993 Proceedings of the 43rd Electronic Components and Technology Conference
Conference Location: Orlando, FL, USA Conference Date: 19930601-19930604
E.I. Conference No.: 18894
Source: Proceedings - Electronic Components and Technology Conference 1993. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. p 396-404
Publication Year: 1993
CODEN: PECCA7 ISSN: 0569-5503 ISBN: 0-7803-0794-1
Language: English
Abstract: A high pin count, high performance PGA has been developed for next-generation ASIC devices which apply half micron BiCMOS technology and have a maximum usable gate count of 300k. In view of the advances in CMOS and BiCMOS ULSI technologies, high performance **packages** are required. This new **package** has been designed with due consideration of all **packages** functions. **Packages** for highend devices need to satisfy the following requirements: high **electrical** performance, low thermal resistance and high pin count in keeping with easy routing of PWB. The body size of the developed **package** is 60 multiplied by 60 mm**2. Surface mount type pin **joint** was adopted to realize high wiring density of a printed wiring board. This **package** has 820 pins with 50mil pitch, and 5 rows. A small pin diameter of 0. 2mm and a short pin length of 3.0mm were used for surface mounting. The maximum available **bonding pad** count of the **die** is 812 with 80 mu m pad pitch. The inner bonding pitch of the **package** is 90 mu m. To achieve the narrow pitch and high pad count of the bonding from the **dies** to the **package**, highly accurate TAB technology was applied to **die** assembly. A fine metallization pitch of 90 mu m was formed on the ceramic PGA. The thermal resistance from **die** to air is lower than 1.5 degree C/W at 1m/s air flow velocity. This low thermal resistance was achieved by a CuW heat spreader equipped with an optimized heat sink. An omnidirectional heat sink was developed which has large heat transfer coefficient at slow air flow. Ultra large-scale BiCMOS devices which have power dissipation of as much as 20W can be housed in this **package**. Great care was taken with respect to the **electrical** design of the **package**. The **package** keeps flexibility of the signal interface types and matches system requirements. Two power supply voltages for the device are available to apply TTL (CMOS) and ECL interfaces by the layer design. The characteristic impedance was controlled at 60 Omega . The

electric parameters of the **package** were quantified. The measured cut-off frequency (-3dB) is kept to 1.25GHz including the TAB **lead**. **Electrical** characteristics of the **package** realize complete transmitted signal form of more than 100MHz. (Author abstract)

24/3,AB/42 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)


02802628
E.I. Monthly No: EI8910103620
Title: Single point TAB - a bonding solution for high density **chips**.
Author: Kelly, Greg
Corporate Source: Orthodyne Electronics Corp, Costa Mesa, CA, USA
Source: Surface Mount Technology v 3 n 4 Aug 1989 p 16-18
Publication Year: 1989
CODEN: SMTEEL ISSN: 0893-3588
Language: English
Abstract: New tape automated bonding (TAB) equipment, which has been developed to overcome the spacing constraints of wirebonding that limit **package** and device design is reported. TAB is capable of 2 multiplied by 2 mil **bonding pads** with 4 mil centerline spacing its low profile minus 2 to 4 mils above the **chip** - make it a common choice for smart cards, watches, credit card calculators, and read/write head circuitry. Additionally, because the size of a high I/O **chip** is often determined by the **peripheral** length needed for **bond pads**, a reduction in **bond pad** pitch from 6 to 4 mils for a pad-limited **chip** can result in a **chip** area reduction of about 56 percent.

24/3,AB/43 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)


02026815
E.I. Monthly No: EI8610102117
E.I. Yearly No: EI86105628
Title: COPPER-WIRE BONDING OF PLASTIC-MOLDED SEMICONDUCTOR **PACKAGES**.
Author: Hirota, Jitsuho; Machida, Kazumichi
Corporate Source: Mitsubishi Electric Corp
Source: Mitsubishi Electric Advance v 35 Jun 1986 p 25-28
Publication Year: 1986
CODEN: MEADD4 ISSN: 0386-5096
Language: ENGLISH
Abstract: Under high-temperature conditions, gold from gold-wire bonds generally employed in plastic-molded semiconductor **packages** diffuses into the aluminum **bonding pad** of the silicon **chip**, forming compounds that result in bond failure. Fluctuations in the price of gold hinder cost control. The changeover to an alternative material would eliminate these problems and hence, basic studies on copper, aluminum, and silver, their impurities, and their applications in wire-bonding processes have been underway for several years. An additional advantage of copper over gold - lower rate of diffusion into aluminum **bonding pads**

- led us to develop copper-wire bonding technologies on bonding machines employed for gold-wire bonding. These technologies led to the development of a power supply for the arc discharge used in ball formation, a heated capillary tip for use in ball bonding, and aluminum **bonding pads** of controlled hardness. 7 refs.

24/3,AB/44 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci


10258285 Genuine Article#: 504UQ Number of References: 6
Title: A new concept of 3-dimentional multilayer-stacked system-in-**package** for software-defined-radio (ABSTRACT AVAILABLE)
Author(s): Tsubouchi K (REPRINT) ; Yokoyama M; Nakase H
Corporate Source: Tohoku Univ,Res Inst Elect Commun,Sendai/Miyagi 9808577/Japan/ (REPRINT); Tohoku Univ,Res Inst Elect Commun,Sendai/Miyagi 9808577/Japan/
Journal: IEICE TRANSACTIONS ON ELECTRONICS, 2001, VE84C, N12 (DEC), P 1730-1734
ISSN: 0916-8524 Publication date: 20011200
Publisher: IEICE-INST ELECTRONICS INFORMATION COMMUNICATIONS ENG, KIKAI-SHINKO-KAIKAN BLDG MINATO-KU SHIBAKOEN 3 CHOME, TOKYO, 105, JAPAN
Language: English Document Type: ARTICLE
Abstract: In the present GHz-clock high-density LSI, a design of signal lines is getting so critical that the transmission line analysis should be introduced to signal line design. This **leads** to the complex design of line structure and i/o drivers including impedance matching. Our target is to implement a system-in-**package** (SiP) for software-defined-radio (SDR) The SiP operates tip to 10GHz, and requires a compact and high-density packaging technology with a simple signal wiring design. In this paper, we propose a new concept of 3-D multilayer-stacked SiP. The new 3-D packaging concept includes (1) design guideline for interconnection lengths. (2) bridging register circuits in LSI **chips**. (3) flip-**chip** microbump bonding technology of **chips** onto system-buildup printed wiring boards (PWB), (4) multilayer-stacked 3-D **package** of several sets of **chips** and PWB. and (5) 100-mum-diameter bumps at **peripheral** region of PWB as vertical via-bump bus lines. A critical interconnect length, in which interconnect wiring is treated as a conventional RC line, is discussed for wiring design. Both wiring lengths in LSI **chips** and that among **chips** corresponding to total thickness of vertical bus lines are designed to be shorter than the critical length. The key points of the 3-D pack-age for GHz signal transfer are a delay guarantee due to limitation of line length and separation between local lines in a **chip** and a bus line among **chips**.

24/3,AB/45 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus


03214520 JICST ACCESSION NUMBER: 97A0632019 FILE SEGMENT: JICST-E
Effect of Mold Resin on Reliability in Gold-Aluminium Bonding.
ONO YASUHIDE (1); SHIMIZU ISAO (1)
(1) Kumamoto Univ.
Yosetsu Gakkai Ronbunshu(Quarterly Journal of the Japan Welding Society),

1997, VOL.15,NO.2, PAGE.383-388, FIG.10, REF.7
JOURNAL NUMBER: Y0413AAA ISSN NO: 0288-4771
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: In semiconductor devices the gold wire **bonding** to aluminium **pads** is a widely used bonding practice. The reliability of bond strength exerts a strong influence on that of **IC** or LSI. Voids formed in gold-aluminium intermetallic compounds are known to degrade the long-term reliability of gold wire **bonds** to aluminium **pads**. In this reliability, the annealing envirenment has great influence on the behavior of this voiding as well as the intermetallic formation. The influence of annealing condition for gold-aluminium bonds was investigated comparing with the **encapsulated** condition and decapped condition. Great differences were found between two conditions. In the **case** that initial shear strength is high, shear strength was high even after annealling in 200C-1000hr for decapped devices. However, in the **case** of **encapsulated** condition shear strength was degraded after annealling in 200C-100hr. In the **case** of **encapsulated** condition, intermetallic compounds was corroded by bromine included in resin. And this corroded compound degraded gold-aluminium bonding. On the other hand, in the **case** that initial shear strength is low, shear strength became low after annealling in 200C-100hr for both conditions. In conclusion, shear strength was degraded after annealling in 200C-100hr for **encapsulated** condition, irrelevant to bonding conditions. (author abst.)

24/3,AB/46 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus


02267300 JICST ACCESSION NUMBER: 94A0789390 FILE SEGMENT: JICST-E
Special issue : New-type **packages** and problems of packaging technology. Flip-**chip** mounting using electroconductive adhesive.
TOMURA YOSHIHIRO (1); BESSHO YOSHIHIRO (1); ONO MASAHIRO (1); TSUKAMOTO KATSUHIDE (1); ISHIDA TORU (1); OMOYA KAZUNORI (2); OBAYASHI TAKASHI (2)
(1) Matsushitadenkisangyo Zairyodebaisuken; (2) Matsushita Technoresearch, Inc.
Denshi Zairyo(Electronic Parts and Materials), 1994, VOL.33,NO.9, PAGE.22-29, FIG.10, TBL.5, REF.11
JOURNAL NUMBER: F0040AAH ISSN NO: 0387-0774
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: This paper describes the flip-**chip** packaging technology by the stud **bump bonding** method. Golden 2 stage protrusion electrodes are provided on the LSI **chip**, the electroconductive adhesive is put on the tops of them, and the LSI is mounted on the circuit board in a face down, in order to get **electrical connection**. Afterwards, the junction part is reinforced

mechanically with the epoxy series **encapsulation** resin, and the high reliability can be achieved.

24/3,AB/47 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus


01061008 JICST ACCESSION NUMBER: 90A0454999 FILE SEGMENT: JICST-E
Small-sized pressure senser for absolute pressure with new feedthrough structure.
MATSUMOTO YOSHINORI (1); ESASHI MASAYOSHI (2); SHOJI SHUICHI (2)
(1) Tohoku Univ., Graduate School; (2) Tohoku Univ., Faculty of Engineering
Denki Gakkai Ronbunshi. C(Transactions of the Institute of Electrical Engineers of Japan. C), 1990, VOL.110,NO.4, PAGE.255-262, FIG.12, REF.6
JOURNAL NUMBER: S0810AAN ISSN NO: 0385-4221
UNIVERSAL DECIMAL CLASSIFICATION: 531.78
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: An absolute pressure sensor has reference **cavity** and **electrical** feedthrough from the **cavity**. The reference **cavity** has to be hermetically sealed, but the **electrical** feedthrough at the bonding surface makes small leakage. In this paper, a new feedthrough structure is proposed and is applied to a piezoresistive pressure sensor. A pyrex glass and a silicon are used for this structure. The pyrex glass has fine through-holes engraved by electrolytic discharge drilling. The silicon has the diffused **electrical** feedthrough from the reference **cavity**. The reference **cavity** is hermetically sealed by glass-silicon anodic **bonding**. **Bonding pads** are made by Cr-Cu-Au mask evaporation to the glass holes. **Lead** wires are **connected** to the pads inside the glass hole with conductive epoxy or solder. The advantages of this strucutre are as follows. (1) Reference **cavity** is hermetically sealed without leakage by glass-silicon anodic bonding. (2) Sensor is assembled in small size. (3) **Lead** wires are attached at the opposite side of the diaphragm and strongly enough. The piezoresistive absolute pressore sensor with this structure is small and high performance. This structure is also useful for capacitive absolute pressure sensors. (author abst.)

24/3,AB/48 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs


1697875 H.W. WILSON RECORD NUMBER: BAST95032882
Making the bare-**die** decision
Schrand, Jim; Ried, Rick
Electronic Design v. 43 (May 1 '95) p. 129-30+
DOCUMENT TYPE: Feature Article ISSN: 0013-4872

ABSTRACT: The issues that should be considered before embarking on a **die**-based design are reviewed. A method to reduce the volume taken up by electronic devices is to remove the **package** and place the **ICs** directly on the printed wiring board using a method known as

direct **chip** attach (DCA). It has been demonstrated that the board area consumed by an **IC** can be reduced by 75 percent or more by changing from a conventional **package** to a DCA approach. An important consideration when examining the option of using **die** in a design is the choice of **die**-attach technology. **Chip**-on-board (COB) and flip **chip** are the 2 most common direct-**die**-attach approaches. For flip-**chip die** bonding, the **die** is required to have solder bumps placed on its **bond pads**. For COB, the substrate of the **die** is attached to the board and the **electrical connection** is realized using bond wires.

24/3,AB/49 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal


15591518 PASCAL No.: 02-0293251
CAD Design for area pad transformation
**Microelectronics** : Baltimore MD, 9-11 October 2001
HUANG Yu-Jung; KO Ching-Mai; FU Shen-Li
Department of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan; ASE TEST, Inc., Kaohsiung, 84008, Taiwan
International Society for Optical Engineering, Bellingham WA, United States
International symposium on microelectronics (Baltimore MD USA) 2001-10-09
Journal: SPIE proceedings series, 2001, 4587 610-615
Language: English
As the demand for smaller, lighter, power efficient devices grows, the area array bonding technology are becoming more important for high pin count and high performance **packages**. Ball grid arrays (BGA) and **chip** scale **packages** (CSP) technologies are a major factor in the miniaturization and functionality of today' s co nputi ng and communication products. However, the majority of existing **ICs** are usually designed in a **peripheral** format for wire bonding. Due to area array bonding for bare **die** becomes more prevalent, it is important to have the automatic design methodology for the **peripheral bond pads** to be relocated to area-array format. In this paper, we describe the methodology to solve the problem of redistributing from **bond pads** on periphery of the **IC** to area array of the solder bumps. Several computer aided design cases of the conversion technique from periphery wire-**bond pads** to an area array of pads are presented.



24/3,AB/50 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal


14130030 PASCAL No.: 99-0326173
New receptacle optical modules using ferrule-integrated **chip** carrier with solder-**bump**-**bonded** photonic device: Singlemode-fiber-based high-speed PIN PD receivers
HAYASHI T; TSUNETSUGU H
NTT Opto-electronics Lab, Tokyo, Japan

Journal: IEEE Transactions on Components, Packaging, and Manufacturing Technology Part A, 1998, 21 (4) 592-598
Language: English
A new receptacle optical module is proposed that requires no optical-axis adjustment. In this scheme, coupling a photonic device to a fiber is done basically by simple butt-joining, which is accomplished automatically by solder-**bump bonding** the device onto a platform with an optical fiber glued to a ceramic ferrule. To achieve this coupling, alumina **chip** carriers were fabricated to include a zirconia ferrule (containing a singlemode fiber). The misalignment between the fiber and the solderable patterns on the **chip** carrier was below 5 mu m (with a cumulative distribution of 50%). Prototype MU (IEC standard, IEEE P1355) receptacle receiver modules were demonstrated. By solder-**bump-bonding** the photodiode (PD) onto the **chip** carrier, optical coupling was achieved simultaneously with **electrical connection** to the **chip** carrier. No optical-axis adjustment was required throughout the entire fabrication of the module. The module achieved wide bandwidths up to 1 and 5 GHz, respectively, with the PD's with 180- and 50-mu m-diameter active areas installed inside.

24/3,AB/51 (Item 3 from file: 144)
DIALOG(R)File 144:Pascal


14119472 PASCAL No.: 99-0315289
Conductive polymers for **microelectronic** packaging: **chip** bonding to polymer films
KUECHENMEISTER F; BOETTCHER M; MEUSEL E; MEIER D
Dresden Univ of Technology, Dresden, Germany
Journal: Polymers for Advanced Technologies, 1998, 9 (10-11) 806-811
Language: English
A novel flipchip-like **microelectronic** packaging technology for bonding **integrated circuits** to polymer foils using laser micromachining technique and a wet chemical metallization process of conductive polymers has been developed. This paper will focus on the deposition of polypyrrole onto the aluminum surface and the characterization of the thin film using scanning electron microscopy, auger electron spectroscopy and X-ray photoelectron spectroscopy. The conductive polymer is metallized by copper electroplating for **connecting** the **integrated circuit** to the polyimide foil. **Electrical** measurements were performed on patterned substrates with a layer system consisting of polypyrrole/copper/tin-**lead** deposited on aluminum **bond pads** . The characteristic current/voltage curve shows an ohmic contact behavior which is of fundamental importance for the development of **chip** bonding technology using conductive polymers.

24/3,AB/52 (Item 4 from file: 144)
DIALOG(R)File 144:Pascal


13842401 PASCAL No.: 99-0018643
Simultaneous fabrication of dielectric and **electrical joints** by **wafer** bonding
Micromachined devices and components IV : Santa Clara CA, 21-22 September 1998

DROST A; KLINK G; SCHERBAUM S; FEIL M
FRENCH Patrick J, ed; CHAU Kevin, ed
Fraunhofer - Institute for Solid State Technology, Munich, Germany
International Society for Optical Engineering, Bellingham WA, United States.
Micromachined devices and components. Conference, 4 (Santa Clara CA USA) 1998-09-21
Journal: SPIE proceedings series, 1998, 3514 62-71
Language: English

**Wafer** bonding is a key technology for the fabrication of micro mechanical systems which consist of two or more stacked silicon parts. Among the different bonding methods anodic bonding with an intermediate layer of Pyrex glass offers several advantages concerning the process flexibility and the stability of the bond. To use this technology the sputter deposition process of Pyrex glass was optimized and the anodic bonding process was characterized. A process for a capacitive pressure sensor was designed which included bond frames made out of sputtered glass. The electrical contact from both electrodes to **contact pads** was realized by lateral and vertical feedthroughs. The latter were obtained by an Au - Au thermocompression bond which was simultaneously fabricated with the anodic bond.



24/3,AB/53 (Item 1 from file: 103)
DIALOG(R)File 103:Energy SciTec


04718909 EDB-01-068154
Title: Critical Cleaning Requirements for Flip **Chip Packages**
Author(s): Bixenman, M.; Miller, E.; C (Kyzen Corporation (United States))
Title: Proceedings of Fifth International Joint Symposium on **Microelectronics** and Packing
Conference Title: Fifth International Joint Symposium on Microelectronics and Packing
Conference Location: Seoul (Korea) Conference Date: 24 Apr 2000
Publisher: Seoul (Korea) Korea Institute of Science and Technology
Publication Date: 24 Apr 2000
p 43-55 (119 p)
Report Number(s): ETDE/KR-20136250
Order Number: DE20136250
Language: English
Abstract: In traditional electronic **packages** the **die** and the substrate are interconnected with fine wire. Wire bonding technology is limited to **bond pads** around the **peripheral** of the **die**. As the demand for I/O increases, there will be limitations with wire bonding technology. Flip **chip** technology eliminates the need for wire bonding by redistributing the **bond pads** over the entire surface of the **die**. Instead of wires, the **die** is attached to the substrate utilizing a direct solder connection. Although several steps and processes are eliminated when utilizing flip **chip** technology, there are several new problems that must be overcome. The main issue is the mismatch in the coefficient of thermal expansion (CTE) of the silicon **die** and the substrate. This mismatch will cause premature solder joint failure. This issue can be

compensated for by the use of an underfill material between the **die** and the substrate. Underfill helps to extend the working life of the device by providing environmental **protection** and structural integrity. Flux residues may interfere with the flow of underfill **encapsulants** causing gross solder voids and premature failure of the solder connection. Furthermore, flux residues may chemically react with the underfill polymer causing a change in its mechanical and thermal properties. As flip **chip packages** decrease in size, cleaning becomes more challenging. While **package** size continues to decrease, the total number of I/O continue to increase. As the I/O increases, the array density of the **package** increases and as the array density increases, the pitch decreases. If the pitch is decreasing, the standoff is also decreasing. This paper will present the keys to successful flip **chip** cleaning processes. Process parameters such as time, temperature, solvency, and impingement energy required for successful cleaning will be addressed. Flip **chip packages** will be cleaned and subjected to JEDEC level 3 testing, followed by accelerated stress testing. The devices will then be analyzed using acoustic microscopy and the results and conclusions reported. (author). 8 refs., 14 figs.

24/3,AB/54 (Item 2 from file: 103)
DIALOG(R)File 103:Energy SciTec


04607575 EDB-00-077984
Title: Flip **chip package** technologies capable of dealing with ultrafine pitches
Original Title: Bisai pitch taio furippu **chip** jisso gijutsu
Corporate Source: Fuji Electric Co. Ltd., Tokyo (Japan)
Source: Fuji Jiho (Fuji Electric Journal) v 73:1. Coden: FUJIAS ISSN: 0367-3332
Publication Date: 10 Jan 2000
p 19
Language: Japanese
Abstract: As **electrical** appliances grow smaller, it has become indispensable to establish flip **chip package** technologies for bonding bare **chips** directly onto substrates. Fuji Electric Co., Ltd., has established two bonding methods, the gold **bump** /solder **bonding** method and the solder bump/ACF (anisotropic conductive film) bonding method. While the **lead** pitch is 500[mu]m in the conventional QFP (quad flat **package**) and the like, those in the new methods are 120[mu]m for the gold **bump**/solder **bonding** method and 200[mu]m for the solder **bump**/ACF **bonding** method. In the solder **bump**/ACF **bonding** method, but an extremely little load is imposed on the **chip** during the **package** process. The company intends to combine these flip **chip package** technologies and the BGA (ball grid array) **package** technology, which has been available for some time, into a multi-**chip** modularization technology. (translated by NEDO)

24/3,AB/55 (Item 3 from file: 103)
DIALOG(R)File 103:Energy SciTec

03427577 DE-92-015758; EDB-93-006453
Title: Insulating glass pane
Original Title: Isolierglasscheibe
Author(s)/Editor(s): Gochermann, H.
Patent No.: DE 3801989 A1
Patent Assignee(s): Telefunken Systemtechnik GmbH, Ulm (Germany)
Patent Date Filed: 23 Jan 1988
Publication Date: 27 Jul 1989
([10] p)
Language: German
Abstract: Insulating glass pane for facade components, window and so on. It consists of several glass panes of which at least two enclose an air-filled space. They form the front panes and/or back panes of a building, wintergarden etc., where preferably one pane is designed as a laminated insulating glass pane. In order to utilize the light which enters through the insulating glass pane for generation of electric power, the insulating glass pane has a photovoltaic solar generator. The solar cells of the solar generator are connected by electrically **conductive connectors** and are fastened on a glass pane.
Non-English Abstract: Isolierglasscheibe fuer Fassadenbauelemente, Fenster oder dergleichen bestehend aus mehreren Glasscheiben, von denen mindestens zwei einen luftgefuellten Zwischenraum begrenzen und in bezug auf ein Gebaeude, Wintergarten oder aehnlichen als Vorder- bzw. Rueckscheibe anzusehen sind, wobei vorzugsweise eine Scheibe als Verbundglasscheibe ausgebildet ist. Um das **die** Isolierglasscheibe durchsetzende Licht zur Erzeugung von elektrischer Energie auszunutzen, weist **die** Isolierglasscheibe einen photovoltaischen Solargenerator auf, dessen untereinander durch Verbinder elektrisch leitend verbundene Solarzellen auf einer Glasscheibe befestigt sind.
Abstract Language: Deutsch

24/3,AB/56 (Item 4 from file: 103)
DIALOG(R)File 103:Energy SciTec


02181062 NEDO-87-960247; EDB-88-123797
Author(s): Hara, Kazuya; Takeuchi, Eiichi
Title: Circuit substrate
Patent No.: JP 62-264352
Patent Assignee(s): Casio Computer Co., Ltd., Tokyo, Japan
Patent Date Filed: Filed date 3 Mar 1986
Publication Date: 17 Nov 1987
p 11
Language: Japanese
Abstract: Currently, it is aimed to make a small electronic apparatus as thin as a credit card, but such an aim cannot be achieved by the conventional process that an **integrated circuit** elemental device and **chip** parts are attached in layers on an insulative substrate on which a wiring pattern has been formed and are connected to the above wiring pattern by bonding or soldering. This invention offers a circuit substrate, the thickness of which, including an **integrated circuit** elemental device and **chip** parts, is greatly reduced than that of the conventional substrate. In other words, this invention proposes that its circuit substrate is to consist of an insulative substrate which is formed with the first and the

second openings, the predetermined wiring pattern consisting of a conductive metal foil which is fixed on this substrate, an **integrated circuit** elemental device that is stored in the first opening of the above substrate, its each electrode is connected to the above wiring pattern with a **conductive connector** and at the same time, this connected surface side is coated with insulative resin, and **chip** parts that are stored in the second opening of the above substrate and its electrodes are connected to the above wiring pattern. (20 figs)

24/3,AB/57 (Item 5 from file: 103)
DIALOG(R)File 103:Energy SciTec


00137668 ERA-01-026171; EDB-76-075503
Author(s): Lindberg, F.A.
Title: Hardened hybrid semiconductor **packages**. Task II. Final report, 1 Jan--31 Jan 1975
Corporate Source: Westinghouse Defense and Electronic Systems Center, Baltimore, Md. (USA). Systems Development Div.
Publication Date: May 1975
p 27
Report Number(s): AD-A-010782
Contract Number (DOE): DAAG39-73-C-0216
Language: English
Abstract: The work was performed to develop a radiation hardened packaging technique for packaging a whole round semiconductor **wafer**. The metal which connected the **wafer bonding pads** to the **package** output pins was aluminum which was vapor deposited through a mask on the inside surface of the **package**. One end of each **conductor line** was lifted off the **package** surface to form a beam lead. These beam leads were then ultrasonically bonded to the **wafer bonding pad**

FILE 'WPIX, JAPIO'

L1 14 S (PAEK, JONG OR PAEK, J)/AU

L2 2154676 S (PACKAGE? OR ENCAS##### OR PROTECT? OR CASING OR CASE OR CAVITY OR ENCAPSUL? OR CAPSUL?)

L3 5622 S (S01-G02B5 OR U11-E02 OR V01-A01B)/MC

L4 25669 S (G01R-031/26 OR G01R-031/27 OR H01C-001/02 OR H01C-001/036)/IC

L5 874734 S IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRC UIT)) OR (MICRO)(W)(CIRCUIT OR CHIP OR ELECTRONIC?) OR CHIP OR MICROCIRCUIT OR DICE OR DIE OR LOGIC(W) CIRCUIT OR WAFER OR MICROELECTRONIC?

L6 27598 S (CONTACT? OR BOND###)(2N)(PAD OR PADS OR BUMP OR BUMPS)

L7 154724 S L5 AND ((L2 OR L3 OR L4))

L8 5595 S L7 AND L6

L9 1863 S L8 AND LEAD

L10 399 S L9 AND (ELECTRICAL?)(W)(CONNECT? OR JOIN?)

L11 15 S L10 AND (CONDUCTIVE)(W)(WIRE OR LINE)

L12 3 S L10 AND (CONDUCTIVE)(W)(CONNECTOR)

L13 3 S L12 NOT L11

L14 8 S L10 AND PADDLE

L15 7 S L14 NOT (L11 OR L12)

L16 308 S L8 AND PERIPHERAL

L17 73 S L16 AND (ELECTRICAL?)(W)(CONNECT? OR JOIN?)

L18 2 S L17 AND (CONDUCTIVE)(W)(WIRE OR LINE)

L19 1 S L17 AND (CONDUCTIVE)(W)(CONNECTOR)

L20 41 S L17 AND LEAD

L21 38 S ((L18 OR L19 OR L20)) NOT ((L11 OR L12 OR L13 OR L14 OR L15))

L22 9 S L8 AND (CONDUCTIVE)(W)(CONNECTOR)

L23 65 S L8 AND (CONDUCTIVE)(W)(WIRE OR LINE)

L24 27 S L23 AND (ELECTRICAL?)(W)(CONNECT? OR JOIN?)

L25 12 S L24 NOT ((L18 OR L19 OR L20) OR (L11 OR L12 OR L13 OR L14 OR L15))

L11 ANSWER 1 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 2002-598567 [64] WPIX
DNN N2002-474721 DNC C2002-168951
TI Power semiconductor **package** for electronic products such as personal computer has **chip** mounted on several **leads** and **electrically connected** by **conductive wires**.
DC L03 T01 U11 W01
IN CHOI, Y; NAM, S
PA (CHOI-I) CHOI Y; (NAMS-I) NAM S
CYC 1
PI US 2002074634 A1 20020620 (200264)* 19p
ADT US 2002074634 A1 US 2001-896120 20010702
PRAI KR 2000-78538 20001219
AB US2002074634 A UPAB: 20021007
NOVELTY - The semiconductor **package** (1000) has a **chip** (100) which is mounted on several **leads** (120). Several **conductive wires** (110) **electrically connect** the **leads** to the **bonding pads** (101) provided on top surface of the **chip**. A molding material (105) molds the **leads**, the **chip** and the **conductive wires** such that the outer surface of the grooves of each **lead** is partially exposed.
USE - For electronic products such as personal computer, cellular phone and camcorder, etc.
ADVANTAGE - Reliability of solder joints and the thermal performance are increased by **electrically connecting** the **leads** to the **bonding pads** of the **chip** . Since a **die** pad for mounting a **chip** is not needed, the size of the **package** is reduced and sawing is performed so that occurrence of burr is avoided.
DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the power semiconductor **package**.
**Chip** 100
**Bonding pads** 101
Molding material 105
**Conductive wires** 110
**Leads** 120
Semiconductor **package** 1000
Dwg.3C/9

L11 ANSWER 2 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 2002-582251 [62] WPIX
DNN N2002-461667 DNC C2002-164519
TI **Package** of image sensor device includes **cavity** surface formed on transparent molding compound surface that corresponds to active surface.
DC L03 U11
IN CHIANG, L; HSIAO, C; HUNG, C
PA (CHIA-I) CHIANG L; (HSIA-I) HSIAO C; (HUNG-I) HUNG C
CYC 1
PI US 2002060358 A1 20020523 (200262)* 11p
ADT US 2002060358 A1 US 2001-841855 20010425
PRAI TW 2000-124358 20001117
AB US2002060358 A UPAB: 20020926
NOVELTY - A **package** of an image sensor device has a

**cavity** surface (214) formed on a transparent molding compound surface that corresponds to an active surface (208a). An area of the **cavity** is large enough to cover a **chip** (208) of the image sensor and the **cavity** surface is polished to have a smooth surface.

DETAILED DESCRIPTION - A **package** of an image sensor device comprises a **lead** frame (201), a **die** pad (200), and **leads** located at the periphery of the **die** pad. Each **lead** has inner (202b) and outer **leads** (202a). A **chip** of the image sensor is provided having an active surface and a corresponding back surface (208b). **Bonding pads** (207) are formed on the active surface, and the back surface of the **chip** is adhered on the **die** pad. **Conductive wires** (206) are **electrically connected** from the **bonding pads** to the inner **leads**. A transparent molding compound is provided for **encapsulating** the image sensor **chip**, the **die** pad and the inner **leads**. A **cavity** surface is formed on the transparent molding compound surface (212) that corresponds to the active surface. An area of the **cavity** is large enough to cover the **chip** of the image sensor and the **cavity** surface is polished to have a smooth surface.

USE - For use as a **package** of an image sensor device.

ADVANTAGE - The **cavity** surface of the molding surface can reduce abraded damage on the molding surface during packaging process of the image sensor device of the invention.

DESCRIPTION OF DRAWING(S) - The figure is a schematic diagram of a **package** of an image sensor device of the invention.

**Die** pad 200
**Lead** frame 201
**Leads** 202a-b
**Conductive wires** 206
**Bonding pads** 207
**Chip** 208
Active surface 208a
Back surface 208b
Molding surface 212
**Cavity** surface 214

Dwg.5/11

L11 ANSWER 3 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 2002-291091 [33] WPIX
CR 2002-024917 [74]
DNN N2002-227249 DNC C2002-085293
TI Dual-**dies** packaging structure for device integration, has **lead** frame, first and second **die**, bumping redistribution structure layer, and bonding wires.
DC L03 U11
IN HAN, C; YANG, T
PA (HANC-I) HAN C; (YANG-I) YANG T; (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI US 2001054761 A1 20011227 (200233)* 9p
US 6399421 B2 20020604 (200242)
ADT US 2001054761 A1 Div ex US 1998-210270 19981210, US 2001-797546 20010301; US 6399421 B2 Div ex US 1998-210270 19981210, US 2001-797546 20010301
FDT US 6399421 B2 Div ex US 6313527
PRAI US 1998-210270 19981210; US 2001-797546 20010301

AB US2001054761 A UPAB: 20020704
NOVELTY - A dual-**dies** packaging structure has:
(i) a **lead** frame with a **die** pad and **lead** legs;
(ii) a first and a second **die**, both having front sides with **bonding pads**;
(iii) a bumping redistribution structure layer to redistribute the second **bonding pads** to pseudo-**bonding pads**; and
(iv) bonding wires to connect the first and the pseudo-**bonding pads** to the corresponding **lead** legs with a simple connection layout.
DETAILED DESCRIPTION - A dual-**dies** packaging structure comprises:
(a) a **lead** frame (64) comprising a **die** pad (59) and **lead** legs (62);
(b) a first **die** (42) comprising a first front side (52) having first **bonding pads** (48);
(c) a second **die** (50) comprising a second front side having second **bonding pads**;
(d) a bumping redistribution structure layer (56) on the second front side of the second **die** so as to respectively redistribute the second **bonding pads** to pseudo-**bonding pads**, so that the first **bonding pads** and the pseudo-**bonding pads** with similar functions are closely grouped together; and
(e) bonding wires (40) to **electrically connect** the first **bonding pads** and the pseudo-**bonding pads** to the corresponding **lead** legs with a simple connection layout.
The first and the second **die** are fixed to the **die** pad through its backside.
The **die** pad comprises a first surface that holds the first **die**, and a second surface, opposite the first, that holds the second **die**.
An INDEPENDENT CLAIM is also included for a packaging method for dual-**dies** packaging structure comprising:
(a) providing a first **die**, a second **die** and a **lead** frame;
(b) using a bumping redistribution method to respectively redistribute the second **bonding pads** into third **bonding pads**;
(c) gluing the first **die** and the second **die** on the **die** pad of the **lead** frame respectively at a first and a second surface; and
(d) performing an electrical coupling from the first **bonding pads** and the third **bonding pads** through **bonding** wires.
USE - For device integration.
ADVANTAGE - The dual-**dies** packaging structure uses bumping redistribution to relocate **bonding pad** location so that the relocated **bonding pad** pattern has a match with an unusual **bonding pad** pattern, allowing the **die** to be easily and symmetrically bonded out through bonding wires, avoiding signal delay.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of an integrated **chip**, schematically illustrating a dual-

**dies** packaging structure.
Bonding wires 40
First **die** 42
**Bonding pads** 48
Second **die** 50
First front side 52
Bumping redistribution structure layer 56
**Die** pad 59
**Lead** legs 62
Lead frame 64
**Dwg.3/5**

L11 ANSWER 4 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 2002-266434 [31] WPIX
DNN N2002-206996 DNC C2002-079265
TI Manufacture of semiconductor **package** with stacked **dies** by connecting **conductive wires** between wire **bonding pads**, dispensing bead of adhesive around the periphery of the **dies**, curing, and molding monolithic body of **encapsulant**.
DC A26 A85 L03 U11
IN DICAPRIO, V; GLENN, T P; JUSKEY, F J; LOBIANCO, A J; SHERMER, S G
PA (AMKO-N) AMKOR TECHNOLOGY INC
CYC 1
PI US 6340846 B1 20020122 (200231)* 11p
ADT US 6340846 B1 US 2000-730721 20001206
PRAI US 2000-730721 20001206
AB US 6340846 B UPAB: 20020516
NOVELTY - Semiconductor **package** with stacked **dies** is made by stacking a second **die** on top of a first **die**, connecting **conductive wires** between wire **bonding pads** on respective top surfaces of the two **dies** and the substrate, dispensing a bead of an adhesive around the periphery of the **dies**, curing the first layer and bead of adhesive to harden them, and molding a monolithic body of an **encapsulant**.
DETAILED DESCRIPTION - Manufacture of a semiconductor **package** with stacked **dies** involves providing a substrate having mounted on top of it a first semiconductor **die** (14); stacking a second **die** (16) on top of the first **die**; **electrically connecting conductive wires** between wire **bonding pads** on respective top surfaces of the first **die**, second **die**, and the substrate; attaching a bottom surface of the second **die** to the top surface of the first **die** with a first layer of an adhesive (13) such that the bottom surface of the second **die** is supported above the **conductive wires** connected to the wire **bonding pads** on the first **die** without contacting the wires, and such that the adhesive covers the wire **bonding pads** on the first **die**; dispensing a bead of an adhesive (64) around the periphery of the **dies** and onto the substrate such that the bead of adhesive covers the **bonding pads** on the top surface of the second **die**, to which the ends of the **conductive wires** are connected, and the entire length of the **conductive wires** extends between the periphery of the **dies** and the substrate; curing the first layer and bead of adhesive to harden them; and molding a monolithic body of an

**encapsulant** over the first and second **dies** and the bead of adhesive.

USE - The method is used for manufacturing a semiconductor **package** with stacked **dies**.

ADVANTAGE - The method is simple and inexpensive. It eliminates fracturing of the **dies** during the wire bonding process or as a result of incompatible thermal expansions, and the problem of broken wire bonds as a result of wire sweep.

DESCRIPTION OF DRAWING(S) - The figure is a cross sectional side elevation view into a semiconductor **package**.

First layer of adhesive 13
First **die** 14
Second **die** 16
Bead of adhesive 64
Dwg.6/8

L11 ANSWER 5 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 2002-153689 [20] WPIX
CR 1998-413252 [35]; 2002-238701 [11]
DNN N2002-116839 DNC C2002-047966
TI **Lead** frame for attachment to semiconductor **chip** in **leads**-over-**chip** assembly, comprises electrically insulative material layer bonded to portion of bus bar not connected to active area of semiconductor **die**.
DC A85 L03 U11
IN COURTENAY, R W
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 6255720 B1 20010703 (200220)* 13p
ADT US 6255720 B1 Cont of US 1997-872403 19970610, US 1998-70464 19980430
FDT US 6255720 B1 Cont of US 5780923
PRAI US 1997-872403 19970610; US 1998-70464 19980430
AB US 6255720 B UPAB: 20020508

NOVELTY - A **lead** frame comprises:

(A) a **lead** frame pattern having **leads** including **lead** fingers and a bus bar which has at least a portion of its lower surface for insulative attachment to at least a portion of the active surface of a semiconductor **die**; and

(B) a layer of electrically insulative material bonded to at least a portion of the upper surface of the bus bar.

DETAILED DESCRIPTION - A **lead** frame for **electrical connection** to a semiconductor **die** (12) which has an active surface (14) having **bond pads** (16) comprises a **lead** frame pattern having **leads** (18) including **lead** fingers (18A) and a bus bar (20). The bus bar has at least a portion of its lower surface for insulative attachment to at least a portion of the active surface of the **die**. A layer of electrically insulative material is bonded to at least a portion of the upper surface of the bus bar, portions of the upper surface of the bus bar for connecting to **bond pads** and portions of the upper surface of the bus bar insulated from the **die**. The layer of electrically insulative material bonded to at least a portion of the upper surface of the bus bar comprises tape, hardenable fluid, or paste.

INDEPENDENT CLAIMS are also included for:

(A) a method for making a **lead** frame for conductive bonding to a semiconductor **die** comprising forming a **lead** pattern on a conductive metal, bonding a layer of electrically insulative

material to a portion of the upper surface of the conductive metal which is configured to comprise a portion of bus bars, and removing the electrically insulative material from wire bonding areas (44) on the upper surface of the bus bars; and

(B) a semiconductor assembly comprising a semiconductor **die**, a first layer of insulative material (24) covering a portion of the active surface of the **die**, the **lead** frame, **conductive wires** (34, 42) connecting **bond pads** to **lead** fingers and connecting **bond pads** to conductive bus bars, and a second layer of electrically insulative material (50) secured to at least a portion of the upper surface of the conductive bus bars.

USE - For attachment to semiconductor **chip** in **leads**-over-**chip** (LOC) assembly.

ADVANTAGE - The method provides an improvement in the construction of semiconductor devices. It avoids inadvertent shorting of the wires to the bus bars. Looping heights and wire lengths are reduced so that subsequent wire sweep during **encapsulation** is avoided.

DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of a semiconductor device of the invention.

Semiconductor **die** 12
Active surface 14
**Bond pads** 16
**Leads** 18
**Lead** fingers 18A
Bus bar 20
First layer of insulative material 24
**Conductive wires** 34, 42
Wire bonding areas 44
Second layer of electrically insulative material 50

Dwg.1/5

L11 ANSWER 6 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 2002-136757 [18] WPIX
TI Multi **chip package**.
DC U11 V04
IN AHN, S H; JUNG, Y D; LEE, C U
PA (SMSU) SAMSUNG ELECTRONICS CO LTD
CYC 1
PI KR 2001039115 A 20010515 (200218)* 1p
ADT KR 2001039115 A KR 1999-47364 19991029
PRAI KR 1999-47364 19991029
AB KR2001039115 A UPAB: 20020319

NOVELTY - A multi **chip package** is to broaden a selecting range of a semiconductor **chip** by forming a multi **chip package** with semiconductor **chips** having similar size and to reduce a fabrication cost.

DETAILED DESCRIPTION - A multi **chip package** comprises two horizontally arranged semiconductor **chips** having similar size. A **lead**(130,135) is mounted to a predetermined part of top surface of each semiconductor **chip** for **electrically connecting** an exterior terminal to the semiconductor **chip**. A **conductive wire** (140,145) electrically conducts the semiconductor and the **leads**. A moulding product(150) surrounds the semiconductor **chip**, the **conductive wire** and the **lead** to **protect** them from exterior environment. A **bonding**

**pad electrically connected** to the **lead** by the **conductive wire** is in series arranged in one end of top surface of the semiconductor **chip** along a longitudinal direction of the semiconductor **chip**. When two semiconductor **chips** are horizontally arranged, the **bonding pads** formed on the **chips** are symmetrical with respect to each other. The **leads** are attached to a part of top surface of each semiconductor **chip** displaced from the **bonding pad**. A cut groove(155) is formed to individually separate two semiconductor **chips** on which the molding product is formed.
Dwg.1/10

L11 ANSWER 7 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 2002-082046 [11] WPIX
DNN N2002-061092 DNC C2002-024731
TI Electronic **package** for information handling systems, comprises circuitized substrate, thick planar heat sink, electrical conductors, first semiconductor **chip**, and second semiconductor **chip** coupled to first.
DC L03 U11
IN HORTON, R R; LANZETTA, A P; MILEWSKI, J M; MOK, L S; MONTOYE, R K; SHAUKATULLA, H
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6326696 B1 20011204 (200211)* 11p
ADT US 6326696 B1 US 1998-18698 19980204
PRAI US 1998-18698 19980204
AB US 6326696 B UPAB: 20020215
NOVELTY - An electronic **package** comprises:
(i) a circuitized substrate with a **cavity** that passes through the substrate;
(ii) a thick planar heatsink having another **cavity**;
(iii) electrical conductors;
(iv) a first semiconductor **chip** in the **cavities**, directly connected to the conductors and thermally coupled to the heat sink; and
(v) a second semiconductor **chip** electrically coupled to the first semiconductor **chip**.
DETAILED DESCRIPTION - An electronic **package** comprises:
(a) a circuitized substrate (12) with a first and a second surface, and having a first **cavity** (14) that passes completely through the substrate;
(b) a thick planar heatsink (32) having a second **cavity**, and is bonded to the second surface of the substrate with the second **cavity** overlapping at least partially the first **cavity**;
(c) electrical conductors (24) positioned on the first surface of the circuitized substrate, and at least some are located about the periphery of the first **cavity**;
(d) a first semiconductor **chip** (16) positioned within the first and second **cavities**, directly **electrically connected** to at least some of the conductors and thermally coupled to the planar heatsink; and
(e) a second semiconductor **chip** which is positioned on and electrically coupled to the first semiconductor **chip**, and has an outer surface coplanar with the first surface of the substrate.
USE - For information handling systems (computer) field.

ADVANTAGE - The electronic **package** has at least two semiconductor **chips** that are electrically coupled, with one also electrically coupled to and positioned within a **cavity** in a substrate. The **package** also facilitates positioning the **chips** relative to **bonding pads** located on a first surface of the substrate. It is readily adapted for subsequent placement and coupling to a separate conductive substrate, i.e. printed circuit board.

DESCRIPTION OF DRAWING(S) - The figure shows a cross section of an electronic **package** where a heatsink is utilized.

Circuitized substrate 12

**Cavity** 14

First semiconductor **chip** 16

Electrical conductors 24

Heatsink 32

Dwg.2/6

L11 ANSWER 8 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 2002-024917 [03] WPIX
CR 2002-291091 [07]
DNN N2002-019227 DNC C2002-006882
TI Dual-**dies** packaging structure includes bumping redistribution structure layer located on second **die**.
DC L03 U11
IN HAN, C; YANG, T
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI US 6313527 B1 20011106 (200203)* 8p
ADT US 6313527 B1 US 1998-210270 19981210
PRAI US 1998-210270 19981210
AB US 6313527 B UPAB: 20020524

NOVELTY - A dual-**dies** packaging structure includes a bumping redistribution structure layer located on second front side of second **die** so as to redistribute second **bonding pads** to pseudo-**bonding pads**, which have proper locations to functionally match first **bonding pads**. The first **bonding pads** and the pseudo-**bonding pads** having similar function are closely grouped together.

DETAILED DESCRIPTION - A dual-**dies** packaging structure comprises **lead** frame (64) having a **die** pad (59) and **lead** legs (62). First (42) and second **dies** (50) comprising first and second front sides having first (48) and second **bonding pads** (58) are fixed to the **die** pad through their backside, respectively. The **die** pad comprises a first surface used to hold the first **die**, and a second surface opposite the first surface for holding the second **die**. A bumping redistribution structure layer (56) is located on the second front side of the second **die** so as to redistribute the second **bonding pads** to pseudo-**bonding pads**, which have proper locations to functionally match the first **bonding pads** . The first **bonding pads** and the pseudo-**bonding pads** having similar function are closely grouped together. Bonding wires (40) are put on to **electrically connect** the first **bonding pads** and the pseudo-**bonding pads** to the corresponding **lead** legs with a simple connection layout.

USE - As dual-**dies** packaging structure.

ADVANTAGE - Two **dies** are **packaged** in one **die** pad so that the packaging density is increased. Using the bumping redistribution structure layer fabricated in a low fabrication cost, the **packaged chip** is at least double its capability. The dual-**dies** packaging structure is achieved without a need of redesign a mirror **die**. Since the bumping redistribution structure layer is formed with a compact space, the line length difference between the original **bonding pad** and the pseudo-**bonding pad** to the **lead** leg is short, the signal time delay is effectively avoided. The bumping redistribution structure layer is not limited by the dimension of the **die** pad. The structure can also be applied to two different **dies**, or even for greater than two **dies**.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of an **Integrated Circuit chip**.

Bonding wires 40
**Dies** 42, 50
**Bonding pads** 48, 58
Bumping redistribution structure layer 56
**Die** pad 59
**Lead** legs 62
**Lead** frame 64

Dwg.3/5

L11 ANSWER 9 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 1999-556908 [47] WPIX
DNN N1999-412781
TI **Lead** structure in **chip** size semiconductor **package** - has curved **lead** with its flat portion fixed on another **lead** on pad, and its curved portion projected outside molding section.
DC U11
IN HUR, K R; HUH, G R; HUR, K
PA (GLDS) LG SEMICON CO LTD; (HYUN-N) HYUNDAI MICROELECTRONICS CO LTD; (HYUN-N) HYUNDAI ELECTRONICS IND CO LTD
CYC 3
PI JP 11243172 A 19990907 (199947)* 5p
KR 99049144 A 19990705 (200037)
KR 253376 B1 20000415 (200124)
US 6225558 B1 20010501 (200126)
ADT JP 11243172 A JP 1998-351132 19981210; KR 99049144 A KR 1997-68007 19971212; KR 253376 B1 KR 1997-68007 19971212; US 6225558 B1 US 1998-93724 19980609
PRAI KR 1997-68007 19971212
AB JP 11243172 A UPAB: 19991116
NOVELTY - **Lead** (33) formed on the upper surface of semiconductor **chip** (31) at its both sides, is **electrically connected** with **bonding pads** of semiconductor **chip** by **conductive wire** (37). Another **lead** (35) has flat portion fixed on the **lead** (33) while its curved portion extends towards upper side of **chip** and rests on molding unit (39) which seals the **lead** (33). DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **chip** size semiconductor **package** manufacturing method.

USE - In **chip** size semiconductor **package**.

ADVANTAGE - Prevents bending of **lead** and enables reliable mounting on PCB. Moreover heat dissipation is also effected as curved

**lead** is exposed outside. DESCRIPTION OF DRAWING(S) - The figure shows cross-sectional view of **chip** size semiconductor **package**. (31) Semiconductor **chip**; (33,35) **Leads** ; (37) **Conductive wire**; (39) Molding unit.
Dwg.1/5

L11 ANSWER 10 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 1999-152966 [13] WPIX
DNN N1999-110239
TI **Lead** frame for mounting semiconductor **chip** - has interdigitated signal and ground **leads** with high frequency **leads** which are adjacent corners and shielded by ground **leads** on either side.
DC U11 U14
IN SATO, K
PA (NIDE) NEC CORP
CYC 1
PI US 5869898 A 19990209 (199913)* 8p
ADT US 5869898 A US 1997-847500 19970425
PRAI US 1997-847500 19970425
AB US 5869898 A UPAB: 19990331
The **lead** frame (11) includes a conductive **die** pad (10a) fixed to the bottom surface of a semiconductor **chip** (10) sealed in an insulating **package** (12). A number of first conductive ground **leads** (11c,11e,11j,11n,11p) are integral with the **die** pad and project from opposite sides of the insulating **package**. At least two second signal **leads** (11b,11d,11f) are separated from the **die** pad and project from a first side of the **package** and at least two third signal **leads** (11k,11m,11o) are separated from the **die** pad and project from a second side of the **package**.

The second **leads** are interdigitated between at least two first **leads** and the third **leads** are interdigitated between at least a different two first **leads**. A first high frequency **lead** (11g) is separate from the **die** pad and is positioned on the first side of the **package** adjacent a first corner. A second high frequency **lead** (11i) is separate from the **die** pad and is positioned on the second side of the **package** adjacent a second corner. The two high frequency **leads** are electrically shielded against RF radiation by pairs of the first conductive **leads** on either side of them. One **lead** of each of the shielding pairs are **electrically connected** together. **Conductive wires** connect the **leads** to **bonding pads** on the top surface of the **chip**.

USE - For a semiconductor **integrated circuit** device for processing a microwave signal, e.g. a monolithic microwave **integrated circuit** (MMIC).

ADVANTAGE - Achieves good electrical isolation for the high frequency **leads** in the RF band. Allows the **chip** to operate at high frequencies (over 10 GHz) without sacrificing the yield in the assembling work between the **lead** frame and the **chip**.
Dwg.4/5

L11 ANSWER 11 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 1998-413252 [35] WPIX
CR 2002-153689 [45]; 2002-238701 [11]

DNN N1998-334356 DNC C1998-129265
TI **Lead** over **chip** assembly - has bus bars covered by insulator while leaving bonding areas un-obstructed so that bond wires are bonded with shorter wire and lower loop.
DC A85 L03 U11
IN COURTENAY, R W
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 5780923 A 19980714 (199835)* 13p
ADT US 5780923 A US 1997-872403 19970610
PRAI US 1997-872403 19970610
AB US 5780923 A UPAB: 20020508
Semiconductor assembly comprises: (a) a semiconductor **die** having an active surface with an array of **bond pads** on it; (b) a first layer of insulating material covering part of the active surface of the semiconductor **die** and adhesively bonded to it; (c) a **lead** frame, a part of which is attached to part of the first layer of insulating material, and having a number of conductive **leads** including inwardly extending **lead** fingers, outwardly extending terminal portions, and at least one conductive bus bar for **electrical connection** to at least one **bond pad** of the array of **bond pads**, the bus bar interposed between a **bond pad** of the **bond pads** of the semiconductor **die** and one of the **leads** of the **lead** frame; (d) at least one **conductive wire** connecting at least one of the array of **bond pads** to at least one of the **lead** fingers, the **conductive wire** spanning a portion of the bus bar; (e) at least one **conductive wire** connecting at least one of the array of **bond pads** to the bus bar; and (f) a second layer of electrically insulating material secured to the part of the upper surface of the bus bar spanned by the wire, the second layer of insulating material is applied to the bus bar as one of a tape.

The second layer of insulating material is applied as a tape, and is either polyimide, epoxy, acrylic or silicone, preferably a polyimide having high irradiation blocking properties, most preferably ''Kapton'' (RTM: DuPont). The second insulating includes a layer of adhesive on one surface, to bond it to the bus bar, e.g. polyimide, epoxy, acrylic or silicone.

USE - **Lead** over **chip** assembly.

ADVANTAGE - Bond wires which span the bus bars may be bonded with a shorter wire and a lower loop, without the danger of shorting to the bus bars. Harmful wire sweep in the **encapsulation** step is reduced.
Dwg.1/5

L11 ANSWER 12 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 1998-263559 [24] WPIX
CR 1993-251034 [32]
DNN N1998-207839
TI **Lead**-on-**chip** semiconductor device - has **leads** with on-**chip** portions which are electrically coupled to peripheral **bond pads** by **conductive wires** and off-**chip** portions.
DC U11
IN AFSHAR, D D; BIGLER, C G; CASTO, J J; MCSHANE, M B
PA (MOTI) MOTOROLA INC
CYC 4

PI EP 843356 A2 19980520 (199824)* EN 8p
R: DE FR GB IT
EP 843356 B1 20020807 (200259) EN
R: DE FR GB IT
ADT EP 843356 A2 Div ex EP 1993-101062 19930125, EP 1998-102613 19930125; EP 843356 B1 Div ex EP 1993-101062 19930125, EP 1998-102613 19930125
FDT EP 843356 A2 Div ex EP 554742; EP 843356 B1 Div ex EP 554742
PRAI US 1992-829870 19920203
AB EP 843356 A UPAB: 20020916
The **lead**-on-**chip** semiconductor device (70) comprises a semiconductor **chip** (12) having a periphery and an active surface, which has a centreline (A-A) which intersects two opposing sides of the **chip**, a number of **bond pads** (14) formed on the active surface of the **chip** along at least two sides of the periphery, and a number of **leads** (24) having portions which overlie the active surface of the **chip** and interspersed with the number of **bond pads**. Each **lead** of the number of **leads** comprises an on-**chip** portion (36,38) which is electrically coupled to at least one of the number of **bond pads** and which extends from the periphery of the **chip** toward the centreline of the **chip** , and an off-**chip** portion (38) which extends from the periphery of the **chip** away from the **chip**.

The on-**chip** portions of the **leads** are wire bonded to the **bond pads**, and the on-**chip** portion of at least one **lead** of the number of **leads** is configured to be forked with one branch of the forked **lead** lacking a direct wire bond connection to a **bond pad**. The on-**chip** portion of each **lead** comprises an **electrical connection** portion (36) located adjacent to the periphery of the **chip** which receives a wire bond, and an extension portion (38) which extends from the **electrical connection** portion toward the centreline of the **chip**, where the extension portion lacks a wire bond and is provided to improve adhesion between the **chip**, the **lead**, and a moulded **package** body. The **chip** periphery comprises four sides and at least one **bond pad** is positioned along each of the four sides.

ADVANTAGE - Provides **chip** design flexibility, exhibits improved adhesion between leadframe, semiconductor **chip** adhesion tape and moulded resin packaging material.
Dwg.3/3

L11 ANSWER 13 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 1993-337969 [43] WPIX
DNN N1993-261186
TI Thermally enhanced semiconductor device esp. with moulded **package** exposing bare silicon - has semiconductor **die** mounted on **lead** frame with one pad opening smaller than **die** so that **die** inactive surface is exposed through opening in **encapsulant** for insertion of heat sink.
DC U11
IN JOINER, B A
PA (MOTI) MOTOROLA INC
CYC 6
PI EP 566872 A2 19931027 (199343)* EN 8p
R: DE FR GB IT

JP 06021276 A 19940128 (199409)
EP 566872 A3 19940511 (199524)
US 5483098 A 19960109 (199608) 7p
ADT EP 566872 A2 EP 1993-104433 19930318; JP 06021276 A JP 1993-115190 19930420; EP 566872 A3 EP 1993-104433 19930318; US 5483098 A Cont of US 1992-871776 19920421, US 1994-326160 19941018
PRAI US 1992-871776 19920421; US 1994-326160 19941018
AB EP 566872 A UPAB: 19931207
The semiconductor device includes a **die** (12) with a number of **bond pads** on an active surface (13). A **lead** frame (10) with **leads** (18) has a mounting surface (15) with a **die** opening smaller than the semiconductor **die**. Part of the **die** inactive surface is bonded to the **lead** frame mounting surface, above the **die** opening, to expose the remainder of the **die** inactive surface.
Multiple **conductive wires** (20) **electrically connect** the **bond pads** to the **lead** frame **leads**. An **encapsulant** forms a **package** body over the **lead** frame, the wires, the **die** edge and active surface, and over the **die** inactive surface area bonded to the **lead** frame mounting surface. The **package** includes an opening (23) to expose the remainder of the **die** inactive surface. The **lead** frame may be flagless, with either **die** active or inactive surface mounted to the **lead** frame **leads**. Pref. a thermally conductive heat dissipation structure (26) is attached to the **die** inactive surface with a thermal grease or adhesive.
ADVANTAGE - Increased **package** crack resistance during printed circuit board mounting.
Dwg.3/5

L11 ANSWER 14 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 1992-064413 [08] WPIX
CR 1992-348654 [42]
DNN N1992-048499 DNC C1992-029500
TI Fabricating improved integrity semiconductor **package** - using polyimide adhesive-coated film holding bending wires against **leads** and bending pads.
DC A85 U11
IN CONRU, W H; IRISH, G H; PAKULSKI, F J; SLATTERY, W J; STARR, S G; WARD, W C; CONRU, H W
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP
CYC 5
PI US 5086018 A 19920204 (199208)*
EP 513521 A2 19921119 (199247) EN 10p
R: DE FR GB
JP 05109801 A 19930430 (199322) 11p
EP 513521 A3 19930714 (199406)
EP 513521 B1 19990630 (199930) EN
R: DE FR GB
DE 69229489 E 19990805 (199937)
ADT EP 513521 A2 EP 1992-105953 19920407; JP 05109801 A JP 1992-80916 19920402; EP 513521 A3 EP 1992-105953 19920407; EP 513521 B1 EP 1992-105953 19920407; DE 69229489 E DE 1992-629489 19920407, EP 1992-105953 19920407
FDT DE 69229489 E Based on EP 513521
PRAI US 1991-694719 19910502

AB US 5086018 A UPAB: 19931006
Semiconductor **package** is formed by placing a **lead** frame (10) having number of **leads** (14) adjacent a major surface of a semiconductor **chip** (12) having input and output **bonding pads** (15) and **electrically connecting** respective **leads** to respective **pads** by **bonding conductive wires** (16) between them. An insulating film (18) having a thermosetting plastic adhesive coating (17) is placed over the **lead** frame and pushed against the **pads** and **bonded leads** so that the adhesive is forced between them and the film is heated to cure the adhesive.
USE/ADVANTAGE - Enables semiconductor **package** to be fabricated with improved mechanical and electrical performance and enhanced reliability. It also enables thinner **packages** to be formed and **chips** to be stacked in a manner such that a stack can be readily disassembled if defective **chips** are found.
2,3/5

L11 ANSWER 15 OF 15 WPIX (C) 2002 THOMSON DERWENT
AN 1989-150943 [20] WPIX
DNN N1989-115306
TI High-density electronic module mfg method - depositing electrically conducting **bonding bumps** on conductive terminals of both access plane and substrate and aligning bumps.
DC U11 U14
IN GO, T C
PA (IRVI-N) IRVINE SENSORS CORP
CYC 12
PI WO 8904113 A 19890505 (198920)* EN 35p
RW: AT BE CH DE FR GB IT LI LU NL SE
W: JP
EP 385979 A 19900912 (199037)
R: AT BE CH DE FR GB IT LI LU NL SE
JP 03501428 W 19910328 (199120)
EP 385979 B1 19930811 (199332) EN 20p
R: AT BE CH DE FR GB IT LI LU NL SE
DE 3787032 G 19930916 (199338)
EP 385979 A4 19910612 (199517)
ADT WO 8904113 A WO 1987-US2746 19871020; EP 385979 A EP 1988-900618 19871020; JP 03501428 W JP 1988-501172 19871020; EP 385979 B1 WO 1987-US2746 19871020, EP 1988-900618 19871020; DE 3787032 G DE 1987-3787032 19871020, WO 1987-US2746 19871020, EP 1988-900618 19871020; EP 385979 A4 EP 1988-900618
FDT EP 385979 B1 Based on WO 8904113; DE 3787032 G Based on EP 385979, Based on WO 8904113
PRAI WO 1987-US2746 19871020
AB WO 8904113 A UPAB: 19950502
The manufacturing method comprises the steps of providing a number of **integrated circuit chips** each with a multiplicity of closely-spaced electrical **leads** at one or more edges. The **integrated circuit chips** are stacked and bonded in a structure with an access plane, with two-dimensional array of closely-spaced electrical **leads**. A number of **conductive lines** and a number of conductive terminals are formed on the access plane in direct or indirect electrical contact with the **chip leads**.

A stack-carrying substrate is adapted to support the stacked **chips** and has formed on a number of **conductive lines** and terminals. The conductive terminals on the access plane are located in matched relationship with conductive terminals on the stack-carrying substrate.

L13 ANSWER 1 OF 3 WPIX (C) 2002 THOMSON DERWENT
AN 2002-048234 [06] WPIX
DNN N2002-035628 DNC C2002-013427
TI Manufacture of **chip**-sized semiconductor **package**, e.g. ball grid array, involves mounting on **chip** an insulative substrate having thermal coefficient of expansion closely matching that of the **chip**.
DC A85 L03 U11 U12
IN GLENN, T P; HOLLAWAY, R D
PA (AMKO-N) AMKOR TECHNOLOGY INC
CYC 1
PI US 6291884 B1 20010918 (200206)* 18p
ADT US 6291884 B1 US 1999-437013 19991109
PRAI US 1999-437013 19991109
AB US 6291884 B UPAB: 20020128
NOVELTY - A **chip**-sized semiconductor **package** is made by mounting an insulative substrate (126) on the top surface of the **chip** (104). The rigid substrate has a thermal coefficient of expansion (TCE) equal to the TCE of the **chip** plus or minus 2.5 ppm/ deg. C.

DETAILED DESCRIPTION - Manufacture of **chip**-sized semiconductor **package** from a **chip** having contacts involves:

(a) mounting an insulative substrate on the top surface of the **chip**;

(b) **electrically connecting** first terminals of the conductors on the substrate to the contacts on the **chip**; and

(c) **encapsulating** the contacts on the **chip**, the first terminals on the substrate, and the **conductive connectors** with a **protective encapsulant**.

The rigid substrate has a thermal coefficient of expansion (TCE) equal to the TCE of the **chip** plus or minus 2.5 ppm/ deg. C.

An INDEPENDENT CLAIM is also included for a **chip**-size semiconductor **package** including a semiconductor **chip**, an insulative substrate, conductors, **conductive connectors**, and a **protective** layer of **encapsulant**.

USE - For producing surface-mounting, **chip**-size ball grid array (CS-BGA), land grid array, and **lead**-less **chip** carrier semiconductor **packages**.

ADVANTAGE - The method reduces manufacturing costs of the **packages** relative to that of individually **packaged chips**. It eliminates the need for a silicone interposer between the substrate and the **chip** otherwise necessary to prevent stress-related problems caused by the difference in the respective thermal expansion and contraction of the **chip** and substrate with changes in temperature. This, further reduces the cost of the **packages**, improves heat transfer from the **chips**, and results in a **package** that is free of thermal-induced stresses.

DESCRIPTION OF DRAWING(S) - The figure shows a perspective view partially in section of a wire-bonded CS-BGA **package** made according to the method.

**Chip** 104

Insulative substrate 126

Dwg.4/19

L13 ANSWER 2 OF 3 WPIX (C) 2002 THOMSON DERWENT
AN 1995-015963 [03] WPIX
DNN N1995-012592
TI Semiconductor **integrated circuit** device sealed in resin - uses semiconductor device adhesive filled in mounting pad insertion concave section.
DC U11
IN UMEHARA, N
PA (TEXI) TEXAS INSTR INC; (TEXI) NIPPON TEXAS INSTR KK
CYC 7
PI EP 628997 A2 19941214 (199503)* EN 23p
R: DE FR GB NL
JP 06350010 A 19941222 (199510) 12p
EP 628997 A3 19950906 (199614)
US 5623123 A 19970422 (199722) 19p
SG 48840 A1 19980518 (199834)
EP 628997 B1 20020410 (200227) EN
R: DE FR GB NL
DE 69430341 E 20020516 (200240)
ADT EP 628997 A2 EP 1994-304221 19940610; JP 06350010 A JP 1993-165248 19930610; EP 628997 A3 EP 1994-304221 19940610; US 5623123 A US 1994-258119 19940610; SG 48840 A1 SG 1996-2657 19940610; EP 628997 B1 EP 1994-304221 19940610; DE 69430341 E DE 1994-630341 19940610, EP 1994-304221 19940610
FDT DE 69430341 E Based on EP 628997
PRAI JP 1993-165248 19930610
AB EP 628997 A UPAB: 19950126
The semiconductor device includes a semiconductor element sealed in a state of being fixed on a mounting pad smaller than the element. A concave part is formed on the mount surface of the pad and is filled with fixing agent. A side surface of the mounting pad is slanted inwardly from the mount surface towards the opposite surface. An additional mounting part is provided to a support pin.

The support pin has a concave part filled with fixing agent. A heater member contacts the fixed element and a bonding inner **lead** part of the **lead** frame and the element.

USE/ADVANTAGE - For device packaging. Reduces warpage or cracking of resin due to avoiding separation between pad and resin. Efficient and stable bonding of **leads**.

Dwg.1/26

L13 ANSWER 3 OF 3 JAPIO COPYRIGHT 2002 JPO
AN 1989-205434 JAPIO
TI SEMICONDUCTOR DEVICE
IN NAKAJIMA KAZUHIRO; KUME TORU
PA NEC CORP
PI JP 01205434 A 19890817 Heisei
AI JP 1988-30235 (JP63030235 Showa) 19880210
PRAI JP 1988-30235 19880210
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1989
AB PURPOSE: To provide a terminal having current capacity larger than that obtainable by using bonding wires, by connecting a connecting pad provided at the center of a semiconductor **chip** with a **package** cap by means of a **conductive connector**.

CONSTITUTION: A connecting pad 9 to be connected with a power supply or the ground is provided at the center of a semiconductor **chip** 2. A plurality of probes (of a metal) 10 are welded or soldered to a metallic

cap 5 and fixed such that they are in contact with the connecting pad 3 at the center of the **chip**. The probes 10 are **electrically connected** to the outside of a **package** directly by the metallic cap 5. **Bonding pads** 1 on the periphery of the **chip** are connected to **leads** of a ceramic base 7 by means of bonding wires 8. The connecting pad 9 is similar in construction to conventional ones but is different in arranged position and dimensions. The probes 10 in contact with the connecting pad 9 may be thicker than the bonding wires. Further, impedance of the supply wiring can be decreased by increasing a number of the probes while increasing the dimensions of the connecting pad 9.

L15 ANSWER 1 OF 7 WPIX (C) 2002 THOMSON DERWENT
AN 2002-544665 [58] WPIX
TI **Lead** frame for semiconductor **package**.
DC U11
IN YOON, H S
PA (CHIP-N) CHIPPAC KOREA CO LTD
CYC 1
PI KR 2002012059 A 20020215 (200258)* 1p
ADT KR 2002012059 A KR 2000-45486 20000805
PRAI KR 2000-45486 20000805
AB KR2002012059 A UPAB: 20020910
NOVELTY - A **lead** frame for a semiconductor **package** is provided to reduce the whole thickness of the **package** to 0.8 millimeter or less, by disposing a **lead** under the **paddle** of the **lead** frame so that a metal wire does not protrude out from the surface of the **paddle**.
DETAILED DESCRIPTION - A semiconductor **chip** is adhered to the bottom surface of the **paddle**(21) positioned in the center. Tie bars(24) are downwardly extended from the corner of the **paddle**. The **lead**(22) is connected to an end portion of each tie bar, and is in parallel with the **paddle**. A protrusion(23) is formed on the bottom surface of the **lead**, and the **bond pad** of the semiconductor **chip** is **electrically connected** to the surface of the **lead**.
Dwg.1/10

L15 ANSWER 2 OF 7 WPIX (C) 2002 THOMSON DERWENT
AN 2000-350487 [30] WPIX
DNN N2000-262643
TI **Lead** frame structure for semiconductor **package** has mesa section in top of **paddle** block, which is coupled with lower **paddle** section through wall.
DC U11
IN TSAI, J
PA (AZIM-N) AZIMUTH IND CO INC
CYC 89
PI WO 2000024056 A1 20000427 (200030)* EN 28p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW
W: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZA ZW
AU 2000012160 A 20000508 (200037)
ADT WO 2000024056 A1 WO 1999-US24609 19991022; AU 2000012160 A AU 2000-12160 19991022
FDT AU 2000012160 A Based on WO 200024056
PRAI US 1998-105521P 19981022
AB WO 200024056 A UPAB: 20000624
NOVELTY - A rectangular **paddle** block (72) with a top surface contacting **die** is electrically isolated from **leads** (90). The mesa section (76) is arranged in the other top surface and is coupled with a lower **paddle** section (75) by a wall. Tie bars (82) are attached to the **paddle** block for supporting a plate. **Contact pads** of a **die** are **electrically**

**connected** to the **leads**.

DETAILED DESCRIPTION - Each **lead** has a bonding post (92) which is connected to a wire. The upper **lead** section is arranged higher than the post and is connected with a central section (86). Several release holes are formed at the corners of the **paddle** block. Mesa sections are arranged opposite the lower **paddle** section and are electrically isolated from the lower **paddle** section. Both top surface of the **paddle** block and the upper mesa section are bonded through wires.

USE - For semiconductor device **packages** used for high frequency circuits.

ADVANTAGE - Reduces the number of grounding wiring required, by providing a mesa section in the **paddle** block. Reduces inductive impedance due to less grounding wires, improving high frequency performance of the device.

DESCRIPTION OF DRAWING(S) - The figure shows a top plan view of the **lead** frame.

**Paddle** block 72
Lower **paddle** section 75
Mesa section 76
Bars 82
Center section 86
**Leads** 90
Bonding post 92
Dwg.3a/12

L15 ANSWER 3 OF 7 WPIX (C) 2002 THOMSON DERWENT
AN 1998-347538 [30] WPIX
CR 1999-337290 [28]; 2000-557483 [40]; 2002-224861 [05]; 2002-291559 [23]
DNN N1998-271229 DNC C1998-107453
TI **Lead** frame design for **integrated circuit package** - uses an extended **lead** finger to provide a power source or ground, a bus bar and a tape connected by an epoxy paste or an adhesive.
DC A85 L03 U11
IN BROOKS, J M; CORISIS, D J
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 5763945 A 19980609 (199830)* 11p
ADT US 5763945 A US 1996-713798 19960913
PRAI US 1996-713798 19960913
AB US 5763945 A UPAB: 20020524

A **lead** frame comprises many **lead** fingers (18) extending towards a semiconductor device opening in the frame, at least one bus bar with a portion extending along the near end of the fingers (20) and a section of tape whose periphery (16) is attached to at least a portion of the near ends of the fingers. Also claimed are a **lead** frame as above including a **die paddle** and a combination of **lead** frame and a semiconductor device.

Preferably, the tape is attached by an epoxy paste, or, a thermosetting or thermoplastic adhesive.

USE - As **lead** frames for **electrical connection** to semiconductor devices

ADVANTAGE - **Bond pads** may be located anywhere on the periphery of the semiconductor device without requiring additional **leads** or tooling changes; device speed is increased.

Dwg.1/4

L15 ANSWER 4 OF 7 WPIX (C) 2002 THOMSON DERWENT
AN 1994-000849 [01] WPIX
DNN N1994-000648 DNC C1994-000343
TI Compact plastics **encapsulated** charge coupled device unit for mass prodn. - comprises semiconductor **chip, lead** frame, thin confining wall of thermosetting polymer, glass cover, metal wires, and cast body e.g for camcorder.
DC A85 L03 U11 U13
IN HUR, K R
PA (GLDS) GOLDSTAR ELECTRON CO LTD; (GLDS) KINSEI ELECTRON KK; (GLDS) GOLDSTAR CO LTD
CYC 4
PI DE 4319786 A1 19931223 (199401)* 7p
JP 06053462 A 19940225 (199413) 5p
TW 222713 A 19940421 (199422)
US 5534725 A 19960709 (199633) 7p
ADT DE 4319786 A1 DE 1993-4319786 19930615; JP 06053462 A JP 1993-126030 19930527; TW 222713 A TW 1993-103391 19930430; US 5534725 A CIP of US 1993-53534 19930429, US 1994-337016 19941107
PRAI KR 1992-10430 19920616
AB DE 4319786 A UPAB: 19940217
The unit has (a) a semiconductor **chip** which has a CCD and which has **contact pads** (1a) and a light receiving section (16); (b) a **lead** frame which is integral with a **chip** mounting plate (2) and **leads** (3) having inner (3a) and outer (3b) connections; (c) a thin confining wall (4) of predetermined height, on the **chip** surface for enclosing the section (16); (d) a glass cover (5) on top of the wall (4) for tightly closing and allowing light passage to the section (1b); (e) metal wires ()6) for **electrically connecting** the **chip contact pads** (1a) to the inner connections (3a) of the **lead** frame; and (f) a cast body (7) for hermetically sealing the **chip** (1) and the inner connections (3a).

Prodn. of the plastics-**encapsulated** CCD unit is also new.

The confining wall (4) pref. comprises a thermosetting polymer which exhibits adhesive properties at the opposite end daces and which is hardened at above 150 deg.C for 1 hr. for bonding to the glass cover (5). The glass cover (5) pref. comprises highly transparent glass with a refractive index of ca. 1.5 and a transmission of at least 90%.

USE/ADVANTAGE - The CCD unit is useful in a camcorder. The design allows simple and inexpensive mass prodn. of compact CCD units by transfer casting using an inexpensive plastics (esp. injection mouldable resin). Dwg.1/4

L15 ANSWER 5 OF 7 WPIX (C) 2002 THOMSON DERWENT
AN 1993-288667 [36] WPIX
DNN N1993-222008 DNC C1993-128860
TI **IC package** configuration for mounting **IC dies** to common **lead** frame - has electrically insulating heat conductive **die**-attach substrate with bonding traces extending to **lead** frame fingers.
DC L03 U11
IN KWON, Y I; LIANG, L H; KWON, Y
PA (VLSI-N) VLSI TECHNOLOGY INC
CYC 19
PI WO 9317455 A2 19930902 (199336)* EN 21p

RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
W: JP KR
JP 06507276 W 19940811 (199436) 9p
US 5365409 A 19941115 (199445) 11p
WO 9317455 A3 19931125 (199514)
ADT WO 9317455 A2 WO 1993-US1490 19930219; JP 06507276 W JP 1993-514969 19930219, WO 1993-US1490 19930219; US 5365409 A Cont of US 1992-839191 19920220, US 1993-71921 19930604; WO 9317455 A3 WO 1993-US1490 19930219
FDT JP 06507276 W Based on WO 9317455
PRAI US 1992-839191 19920220
AB WO 9317455 A UPAB: 19931122
An **IC package** configuration comprises (i) an electrically insulative, heat conductive **die**-attach substrate which is located centrally in a **lead** frame, having bondign fingers fixed adjacent the periphery of a first surfae of the substrate, and which forms a **die**-attach **paddle** for **die** mounting on a central area of the first substrate surface; (ii) electrically conductive bonding traces which extend from the central area of the first substrate surface, such that the **die** overlies the traces while still providing exposed trace portions as intermediate attachment areas for bonding wires extending between **bonding pads** on the **die** and the traces; and (iii) **electrical connections** between the traces and corresponding **lead** frames fingers.
ADVANTAGE - Various **die** sizes can be accommodated without changing the **lead** frame or the conductive traces, so that either a standard **lead** frame of a common non-standard **lead** frame can be used. The substrate allows the entire **die** to be electrically isolated from the **lead** frame, while providing good heat dissipation.
Dwg.4/10

L15 ANSWER 6 OF 7 WPIX (C) 2002 THOMSON DERWENT
AN 1993-095156 [12] WPIX
DNN N1993-072754 DNC C1993-042018
TI Component having conductors on **lead** on **chip** - comprises insulating film on semiconductor **chip** contg. projections.
DC A85 L03 U11
IN LEE, H G
PA (GLDS) GOLDSTAR ELECTRON CO LTD; (LEEH-I) LEE H G
CYC 5
PI DE 4230187 A1 19930318 (199312)* 11p
JP 06169052 A 19940614 (199428) 9p
US 5358906 A 19941025 (199442) 10p
KR 9406083 B1 19940706 (199616)
TW 301045 A 19970321 (199725)
US 5742096 A 19980421 (199823) 10p
ADT DE 4230187 A1 DE 1992-4230187 19920909; JP 06169052 A JP 1992-243295 19920911; US 5358906 A Div ex US 1992-943908 19920911, US 1993-141455 19931022; KR 9406083 B1 KR 1991-15863 19910911; TW 301045 A TW 1992-106880 19920831; US 5742096 A US 1992-943908 19920911
PRAI KR 1991-15863 19910911
AB DE 4230187 A UPAB: 19931122
Component (I) with conductors on a **chip** (LOC) comprises (a) a semiconductor **chip** (51) with several bond marks (52) arranged in the middle of the surface of the **chip**; (b) an insulating film

(53) formed on both sides of the **chip** surface; (c) several inner conductors (54b), each being **electrically connected** to each mark of the **chip**; (d) a housing (56) surrounding the **chip**, insulating film and the conductors; and (e) several outer conductors (54c); each extending from an inner conductor and acting to connect to an outer element outside of the housing.

The novelty is that (i) the **chip** (51) has several tiny projections (57) formed in both sides on its surface; (ii) the insulating film (53) has milled edges on both its upper and lower surfaces; and (iii) each of the inner conductors has a milled edge on both surfaces.

Prodn. of (I) is also claimed.

ADVANTAGE - (I) not only prevents parasitic capacity increasing when lowering the thickness of the insulating film, but also increases the bonding strength between the insulating film and the housing.

1/9

nd

Dwg.1/9

L15 ANSWER 7 OF 7 WPIX (C) 2002 THOMSON DERWENT
AN 1993-095148 [12] WPIX
DNN N1993-072746 DNC C1993-042015
TI **Chip** housing with thin inner **leads** - has reduced vol. of housing body esp. composed of cast epoxide material.
DC A21 A83 L03 U11 U14
IN YOUNG, S K; KIM, Y S
PA (GLDS) GOLDSTAR ELECTRON CO LTD
CYC 3
PI DE 4230030 A1 19930318 (199312)* 21p
JP 05226562 A 19930903 (199340) 10p
US 5619065 A 19970408 (199720) 21p
ADT DE 4230030 A1 DE 1992-4230030 19920908; JP 05226562 A JP 1992-265633 19920909; US 5619065 A Cont of US 1992-940327 19920903, US 1994-308624 19940919
PRAI KR 1991-15864 19910911
AB DE 4230030 A UPAB: 19931113
A semiconductor housing has (i) a **chip** with connection pads on its upper surface; (ii) an insulation layer formed over the upper **chip** surface apart from the regions corresponding to the pads; (iii) inner **leads** with **bonding bumps** at one end for **electrical connection** to the pads; (iv) a housing body enclosing the **chip**, the insulation layer and the inner **leads**; and (v) outer **leads** extending from the other end of the inner **leads** and having a greater thickness then the inner **leads**, being located outside the housing body. The housing is constructed by (a) dicing a **wafer** to form **chips**, each having several connection pads; (b) producing a strip **lead** frame (23) having a **paddle** (23a) on which one **chip** is placed, inner **leads** (23b) sufficiently long for direct bonding to the **chip** pads, and thicker outer **leads** (23c) connected to the inner **leads**; (c) bonding the **chip** onto the **paddle**; (d) forming an insulation layer over the upper **chip** surface except for the pad regions; (e) **electrically connecting** the ends of the inner **leads** to the **chip** pads; (f) enclosing the **chip**, the insulation layer and the inner **leads** upto the outer **leads** with cast material, pref. epoxide; and (g) forming the outer **leads** to a predetermined shape.

L21 ANSWER 1 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 2002-381663 [41] WPIX
DNN N2002-298667
TI Semiconductor **package** has **chip** mounting substrate and **leads** which are exposed to exterior surface of **encapsulated package**.
DC U11
IN BAEK, J S; JUNG, Y S; KOO, J H; LEE, J H; SEO, S M; CHUNG, Y S; KU, J H; PAEK, J S; YEE, J H
PA (AMKO-N) AMKOR TECHNOLOGY KOREA INC; (AMKO-N) AMKOR TECHNOLOGY INC
CYC 2
PI US 2002020907 A1 20020221 (200241)* 14p
KR 2001090378 A 20011018 (200241)
ADT US 2002020907 A1 US 2001-816852 20010323; KR 2001090378 A KR 2000-15304 20000325
PRAI KR 2000-15304 20000325
AB US2002020907 A UPAB: 20020701
NOVELTY - A semiconductor **chip** (2) has **bond pads** (2a) at **peripheral** portion of an active surface (2b), each of which is **electrically connected** to respective **leads** (6). The central surface (4d) of **chip** mounting substrate (4) and each land (6f) of **leads** (6) are exposed in the horizontal plane of the exterior surface (10a) of an **encapsulated package** (10) covering the **chip**.
USE - Semiconductor **package**.
ADVANTAGE - Secures maximum number of **leads** for signal transfer, by **electrically connecting bond pads** to **chip** mounting substrate. Achieves enhancement in heat radiation by extending effective heat radiation passageways.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional side view of semiconductor **package**.
Semiconductor **chip** 2
**Bond pads** 2a
Active surface 2b
**Chip** mounting substrate 4
Central surface 4d
**Lead** 6
Land 6f
**Encapsulated package** 10
Exterior surface 10a
Dwg.2b/5

L21 ANSWER 2 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 2001-548933 [61] WPIX
CR 2001-464313 [50]; 2001-520884 [57]; 2002-065861 [09]; 2002-120893 [16]; 2002-120934 [16]; 2002-518300 [55]
DNN N2001-407699 DNC C2001-163302
TI Formation of plastic carrier by forming matrix of **lead** frames having **die**-attach pad and **leads**, attaching semiconductor **die** to top surface of each pad, and **encapsulating** matrix of **lead** frames in resin material.
DC A85 L03 U11
IN FAN, N; MCLELLAN, N
PA (ASAT-N) ASAT LTD
CYC 1
PI US 6242281 B1 20010605 (200161)* 11p

ADT US 6242281 B1 Div ex US 1998-95803 19980610, US 1999-363249 19990728
PRAI US 1998-95803 19980610; US 1999-363249 19990728
AB US 6242281 B UPAB: 20020903
NOVELTY - A plastic carrier is formed by forming a matrix of **lead** frames having **die**-attach pad and **leads**, attaching a semiconductor **die** to a top surface of each **pad** and wire-**bonding**, and **encapsulating** the matrix of **lead** frames in a resin material exposing the bottom surfaces of the pads and the **leads**.
DETAILED DESCRIPTION - Formation of plastic carrier involves forming a matrix of **lead** frames arranged in a 2-dimensional regular pattern out of a metal strip. Each **lead** frame includes a **die**-attach pad (601) and **leads** disposed in close proximity to the **die**-attach pad. A semiconductor **die** having **bonding pads** is attached to a top surface of each **die**-attach **pad**. **Bond** wires are provided to **electrically connect** each of the **bonding pads** to the top surface of a corresponding **lead**. The matrix of **lead** frames is **encapsulated** in a resin material so that the bottom surfaces of the pads and the **leads** are exposed.
USE - For forming a plastic carrier, such as a saw-singulated leadless plastic **chip** carrier (SSLPCC).
ADVANTAGE - The invention provides a low cost, high density, and high reliability **integrated circuit package** with superb thermal and electrical performances.
DESCRIPTION OF DRAWING(S) - The figure shows a **lead** frame for a double-row SSLPCC.
**Die**-attach pad 601
Tie bars 607a-d
Dwg.6a/8

L21 ANSWER 3 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 2001-373477 [39] WPIX
CR 2001-456804 [45]; 2001-624391 [59]
DNN N2001-273157 DNC C2001-114028
TI Compliant semiconductor **chip package** includes a set of bond ribbons, which are **electrically connected** between the semiconductor **chip** contacts and the terminals on top of a compliant layer.
DC A85 L03 U11
IN FJELSTAD, J; KARAVAKIS, K
PA (TESS-N) TESSERA INC
CYC 1
PI US 6211572 B1 20010403 (200139)* 11p
ADT US 6211572 B1 Provisional US 1995-7128P 19951031, US 1996-739303 19961029
PRAI US 1995-7128P 19951031; US 1996-739303 19961029
AB US 6211572 B UPAB: 20011211
NOVELTY - Compliant semiconductor **chip package** includes a set of bond ribbons, which are **electrically connected** between the semiconductor **chip** contacts and the terminals (175'') on the top surface (147'') of a compliant layer (140'').
DETAILED DESCRIPTION - A complaint semiconductor **chip package** assembly comprises:(a) a semiconductor **chip** having a set of **peripheral chip** contacts on its surface and a central region bounded by the contacts;(b) a first

dielectric **protective** layer containing apertures on the surface of the **chip**, the apertures exposing the **chip** contacts;(c) a compliant layer having sloping **peripheral** edges above the first dielectric layer within the central region of the **chip**; and(d) a set of electrically conductive bond ribbons, each of which is **electrically connected** to a respective **chip** contact. Each bond ribbon extends along the sloping edges to the top surface of the compliant layer and connects to a respective terminal.

An INDEPENDENT CLAIM is also included for a compliant semiconductor **chip package** assembly comprising (a), (b), (c) and (d) as above in which the **peripheral** edge of the compliant layer has a first transition region near the top surface of the compliant layer and a second transition region near the top surface of the first **protective** dielectric layer and the transition regions have a radius of curvature.

USE - None given.

ADVANTAGE - The **package** has fan-in **leads** that permit minimization of the overall **package** size. The compliant layer provides stress relief to the bond ribbons encountered during handling or affixing the assembly to an external substrate. The dielectric layer relives mechanical stresses associated with thermal mismatch of the assembly and substrate materials during thermal cycling. The assembly can be manufactured without using bond wiring tools, since the bond ribbons are patterned and formed during a standard photolithographic stage within the manufacturing process. The manufacturing process is also amenable to simultaneous assembly of a multiplicity of undiced **chips** on a **wafer** or simultaneous assembly of diced **chips** in a processing boat.

DESCRIPTION OF DRAWING(S) - The diagram shows the formation of concave areas in the compliant layer such that the overlying terminals have cup-like depressions useful for accurate placement of solder balls.

Compliant layer 140''

Top surface 147''

Bond ribbon Terminals 175''

Concave areas 310

Dwg.6B/6

L21 ANSWER 4 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 2001-201270 [20] WPIX
DNN N2001-143376
TI Dual **chip IC package** fabrication method for computer, involves mounting pair of **chips** on either sides of a diepad and enclosing the **chips** with molded compound to form single **package**.
DC U11 U14
IN CHEN, E; CHEN, K; JENG, J
PA (AMIC-N) AMIC TECHNOLOGY INC
CYC 1
PI US 6133067 A 20001017 (200120)* 8p
ADT US 6133067 A US 1998-48467 19980326
PRAI TW 1997-118374 19971206
AB US 6133067 A UPAB: 20010410
NOVELTY - A **die** pad (13) and several **package** pins (14) are formed on central and **peripheral** regions of a **lead** frame (10). **Die** attach process is performed so that **chips** are mounted on corresponding sides of **die**

**pad**. Wire **bonding** process is performed, so as to **electrically connect chips** to selected sets of **package** pins. Molding process is performed so as to form molded compound (17) to simultaneously enclose **chips**.

USE - For manufacturing of dual **chip IC package** for use in computers and electronic devices.

ADVANTAGE - Since both **chips** are formed separately, fabrication becomes simple, thus reducing manufacturing cost and increasing yield rate of fabricated **chips**. Allows good symmetry in **package** architecture, thus increasing good yield rate for **IC packages**.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of dual **chip IC package**.

**Lead** frame 10
**Die** pad 13
**Package** pins 14
Molded compound 17

Dwg.3F/3

L21 ANSWER 5 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 2000-634267 [61] WPIX
DNN N2000-470286
TI Terminal arrangement in semiconductor device, has interconnected outer and inner **leads electrically connected** to pad of semiconductor **chip** which has connectors formed on periphery.
DC U11
PA (HITA) HITACHI LTD; (HITA-N) HITACHI MICON SYSTEM KK
CYC 1
PI JP 2000260931 A 20000922 (200061)* 11p
ADT JP 2000260931 A JP 1999-58478 19990305
PRAI JP 1999-58478 19990305
AB JP2000260931 A UPAB: 20001128

NOVELTY - **Package** (4) containing semiconductor **chip** (1) has connectors (4b) formed on periphery. The **package** has interconnected outer and inner **leads** (2a, 2b) **electrically connected** to pad (1b) of semiconductor **chip**. The inner **leads** are connected to **pad** by **bonding** wire.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for manufacturing method of semiconductor device.

USE - For semiconductor device.

ADVANTAGE - Easy exchange of semiconductor device is enabled. Eliminates requirement of mounting substrate has wiring patterns is made to connect the semiconductor **chip** which improves **package** density of device.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of internal structure of semiconductor device.

Semiconductor **chip** 1
Pad 1b
Outer and inner **leads** 2a,2b
**Package** 4
Connectors 4b

Dwg.1/9

L21 ANSWER 6 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1999-031212 [03] WPIX
DNN N1999-024290

TI Wire bonding structure for **IC package** - includes coupling member with **peripheral** wirings and central **cavity** through which semiconductor **chip** is mounted onto base portion of ceramic substrate.

DC U11
IN YOON, S J; YOON, S
PA (HYUN-N) HYUNDAI ELECTRONICS IND CO LTD
CYC 3
PI JP 10294405 A 19981104 (199903)* 4p
KR 98045326 A 19980915 (199939)
US 6051784 A 20000418 (200026)
KR 244708 B1 20000215 (200118)
ADT JP 10294405 A JP 1997-348593 19971203; KR 98045326 A KR 1996-63508 19961210; US 6051784 A US 1997-986896 19971208; KR 244708 B1 KR 1996-63508 19961210
PRAI KR 1996-63508 19961210
AB JP 10294405 A UPAB: 19990122
The structure has a semiconductor **chip** (20) which has **bonding pads** (20a). The semiconductor **chip** is arranged on the base portion of step-shaped opening provided on the surface of a ceramic substrate (12). A wiring (12c) is **electrically connected** to the ceramic substrate.

The substrate has projected out **leads** (12d) that is connected to an external circuit. Another wiring (14a) is formed on the coupling member (14) which **electrically connects** the wiring (12c) formed on the substrate. The semiconductor **chip** is mounted onto the substrate via central **cavity** of the coupling member.

ADVANTAGE - Prevents turbulence generated in path of signal transmission.

Dwg.1/4

L21 ANSWER 7 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1997-185674 [17] WPIX
CR 1996-293294 [30]; 1996-293295 [30]; 1997-185582 [17]; 1997-185659 [17]
DNN N1997-153187
TI Resin **package** insulated semiconductor device for motor drive - has insulated member arranged in small gap such that it does not contact heat dissipation plate.
DC L03 U11
IN NISHIDA, S; SHIBATA, K
PA (ROHL) ROHM CO LTD
CYC 2
PI JP 09045838 A 19970214 (199717)* 11p
US 5666003 A 19970909 (199742) 34p
ADT JP 09045838 A JP 1995-194663 19950731; US 5666003 A US 1995-551925 19951023
PRAI JP 1995-194663 19950731; JP 1994-284080 19941024; JP 1994-284081 19941024; JP 1995-194662 19950731; JP 1995-194664 19950731
AB JP 09045838 A UPAB: 19971021
The device has a semiconductor **chip** (13) mounted onto a **die** pad (12). An inner **lead** (16) is connected with the **chip** electrically by a wire (19). A resin **package** (11) encloses the **lead** and the **chip**. External **leads** (17) are extended from the inner **lead**. Heat emitted by the **chip** is dissipated using a heat dissipation plate (14) provided on the lower surface of the **die** pad.

The inner **lead** is connected to an insulated member (18) set up in a small gap (20) formed between the **lead** and the heat dissipation plate. This member does not contact the circumferential part of the plate.

ADVANTAGE - Raises assembly operation of heat dissipation plate.

Dwg.1/14

L21 ANSWER 8 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1997-185659 [17] WPIX
CR 1996-293294 [30]; 1996-293295 [30]; 1997-185582 [17]; 1997-185674 [17]
DNN N1997-153172
TI Resin packed semiconductor device e.g. power **IC** for motor drive - has **die** pad attached to heat dissipation plate such that small gap is formed to ends of plate.
DC L03 U11
IN NISHIDA, S; SHIBATA, K
PA (ROHL) ROHM CO LTD
CYC 2
PI JP 09045821 A 19970214 (199717)* 8p
US 5666003 A 19970909 (199742) 34p
ADT JP 09045821 A JP 1995-194662 19950731; US 5666003 A US 1995-551925 19951023
PRAI JP 1995-194662 19950731; JP 1994-284080 19941024; JP 1994-284081 19941024; JP 1995-194663 19950731; JP 1995-194664 19950731
AB JP 09045821 A UPAB: 19971021
The device (10) has a semiconductor **chip** (13) mounted to a **die** pad (12). This **chip** is connected to an inner **lead** (15) using a **bonding pad** (17). The **chip** or the **lead** are enclosed in a resin **package** (11). An external **lead** (16) extended from the inner **lead**.

Heat emitted from the **chip** is dissipated using a heat dissipation plate (14) built into the **package**, below the **die** pad. The **die** plate is connected to the plate such that a gap (18) is formed at the ends of the plate.

ADVANTAGE - Raises heat dissipation action. Performs exact bonding between **chip** and **lead**.

Dwg.1/15

L21 ANSWER 9 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1997-185582 [17] WPIX
CR 1996-293294 [30]; 1996-293295 [30]; 1997-185659 [17]; 1997-185674 [17]
DNN N1997-153095
TI Ultrasonic metal plate bonding method - involves reducing ultrasonic vibration energy transferred from ultrasonic generator to second metal plate, based on oscillation state of that plate.
DC L03 U11
IN NISHIDA, S; SHIBATA, K
PA (ROHL) ROHM CO LTD
CYC 2
PI JP 09045737 A 19970214 (199717)* 8p
US 5666003 A 19970909 (199742) 34p
ADT JP 09045737 A JP 1995-194664 19950731; US 5666003 A US 1995-551925 19951023
PRAI JP 1995-194664 19950731; JP 1994-284080 19941024; JP 1994-284081 19941024; JP 1995-194662 19950731; JP 1995-194663 19950731
AB JP 09045737 A UPAB: 19971021

The method involves using a press tool (4) which is coupled with an ultrasonic generator (6) through an ultrasonic horn (5). The lower end surface of a second metal plate (3) is made to press-fit on the upper surface of a first metal plate (2) which is positioned on a support stand (1), using a press tool.

Under the press-fit state, an ultrasonic vibration energy is transferred to the second metal plate through the press tool, by actuating the ultrasonic wave generator and thus the metal plates are joined. The ultrasonic vibration energy transferred to the second metal plate from the generator is reduced based on the oscillation state of the plate.

USE/ADVANTAGE - For bonding metallic heat dissipation plate to undersurface of **bonding pad**, upper surface of semiconductor **chip** and inner **leads**. Prevents high ultrasonic energy from being passed to metal plate, thus avoiding fault generation and to perform good bonding.

Dwg.1/11

L21 ANSWER 10 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1996-293295 [30] WPIX
CR 1996-293294 [30]; 1997-185582 [17]; 1997-185659 [17]; 1997-185674 [17]
DNN N1996-246570 DNC C1996-093529
TI Semiconductor device with semiconductor element e.g. motor driver, power **integrated circuit** - has metal board with small space which overlaps end part of **lead** terminals, connected to under surface of **die** pad directly.
DC L03 U11
IN NISHIDA, S; SHIBATA, K
PA (ROHL) ROHM CO LTD
CYC 2
PI JP 08125093 A 19960517 (199630)* 5p
US 5666003 A 19970909 (199742) 34p
ADT JP 08125093 A JP 1994-284081 19941024; US 5666003 A US 1995-551925 19951023
PRAI JP 1994-284081 19941024; JP 1994-284080 19941024; JP 1995-194662 19950731; JP 1995-194663 19950731; JP 1995-194664 19950731
AB JP 08125093 A UPAB: 19971021
Semiconductor device has a **die** pad (11) sealed in a heat dissipation fin (12) which is mounted on a **package** main part (16). A semiconductor element (10) is fixed by the **die** part. Multiple **lead** terminals (13) arranged on the periphery of the **die** pad are connected to the semiconductor element by a multiple metal thin **leads**.

The semiconductor element and the metal thin **leads** are sealed inside the **package** main part. One end of the **lead** terminals is projected from the **package** main part. A metal board (15) has a small gap for heat dissipation, which overlaps the end parts of the **lead** terminals. The metal board joins directly to the under surface of the **die** pad.

USE/ADVANTAGE - For audio amplification and high speed operation logical element. Reduces thermal resistance of **package**. Improves reliability of wire bonding and heat proof nature.

Dwg.1/4

L21 ANSWER 11 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1996-293294 [30] WPIX
CR 1996-293295 [30]; 1997-185582 [17]; 1997-185659 [17]; 1997-185674 [17]
DNN N1996-246569 DNC C1996-093528

TI Semiconductor device with semiconductor element e.g. motor driver - has metal board with small space which overlaps end part of **lead** terminals and is connected to under surface of **die** pad by ultrasonic wave.

DC L03 U11
IN NISHIDA, S; SHIBATA, K
PA (ROHL) ROHM CO LTD
CYC 2
PI JP 08125092 A 19960517 (199630)* 5p
US 5666003 A 19970909 (199742) 34p
ADT JP 08125092 A JP 1994-284080 19941024; US 5666003 A US 1995-551925 19951023
PRAI JP 1994-284080 19941024; JP 1994-284081 19941024; JP 1995-194662 19950731; JP 1995-194663 19950731; JP 1995-194664 19950731
AB JP 08125092 A UPAB: 19971021
The semiconductor device has a **die** pad (11) sealed in a heat dissipation fin (12) which is mounted on a **package** main part (16). A semiconductor element (10) is fixed by the **die** part. Multiple **lead** terminals (13) arranged on the periphery of the **die** pad are connected to the semiconductor element by a multiple metal thin **leads**.

The semiconductor element and the metal thin **leads** are sealed inside the **package** main part. One end of the **lead** terminals is projected from the **package** main part. A metal board (15) has a small gap for heat dissipation, which overlaps the end parts of the **lead** terminals. The metal board joins directly to the under surface of the **die** pad by ultrasonic wave.

USE/ADVANTAGE - For audio amplification and high speed operation logical element. Improves reliability wire bonding nature. Prevents cracking of **package** main part. Excels in heat proof nature.
Dwg.1/9

L21 ANSWER 12 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1996-209513 [21] WPIX
DNN N1996-175349
TI Tape automated bonding semiconductor **package** - has **die** with several **chip bonding pads** around periphery, several global signal **chip bonding pads** in **die** centre, conductive **leads** extend beyond **die** periphery **electrically connected** by TAB conductive bump to pad.
DC U11
IN EISENSTADT, R E; ROHRS, K D
PA (VLSI-N) VLSI TECHNOLOGY INC
CYC 18
PI WO 9610841 A1 19960411 (199621)* EN 32p
RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
W: JP KR
ADT WO 9610841 A1 WO 1995-US13078 19950928
PRAI US 1994-315366 19940930
AB WO 9610841 A UPAB: 19960529
The **package** includes a semiconductor **die** (18) with a multiplicity of **chip bonding pads** (20) arrayed about the periphery of a surface of the **die**. Several global signal **chip bonding pads** (21) are positioned centrally to the **peripheral chip bonding pads**. Several conductive **leads** extend

beyond the periphery of the **die**. Each **lead** is **electrically connected** by a TAB conductive **bump** to a **bonding pad**.

A **lead** network (17g) of electrically conductive **leads** extend beyond the periphery of the **die**. Each **lead** of the network is **electrically connected** to one other **lead** of the network. The **lead** network is connected to a central global signal **chip bonding pad** and to a **bonding pad** from the group of **peripheral** and central global **bonding pads**.

ADVANTAGE - Allows semiconductor **dies** to be processed into plastic, ceramic, metal, **chip**-on-**chip**, PGA and other **package** types with ease.

Dwg.8/8

L21 ANSWER 13 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1996-087167 [09] WPIX
CR 1996-076913 [08]
DNN N1996-073106
TI Semiconductor **integrated circuit package** for hybrid circuit, multi-**chip** module - has thermal induction plate extending along **encapsulated package** formed from moulded insulator **encapsulating** semiconductor **die** with **leads** and **bonding pad** inner parts.
DC U11
IN MARRS, R C
PA (AMKO-N) AMKOR ELECTRONICS INC
CYC 1
PI US 5485037 A 19960116 (199609)* 21p
ADT US 5485037 A Cont of US 1993-48888 19930412, US 1995-410381 19950327
PRAI US 1993-48888 19930412; US 1995-410381 19950327
AB US 5485037 A UPAB: 19960305

The **package** includes a semiconductor **die**, several **package** signal **leads**, a thermal induction plate, and a moulded electrical insulator. The **die** has electrical circuitry on one surface with several electrical **bond pads** positioned at its **peripheral** edges. Each **lead** has mutually opposite surfaces with an inner portion spaced from and juxtaposed to respective **bond pad** surfaces. The induction plate has a planar section extending in a band to overlay the **package lead** inner portions. The plate also has a band surface adjacent to and electrically isolated from the inner portions.

The **leads** and the **bond pads** are **electrically connected** and the other plate planar section and surface overlay the **die** circuitry surface, the **bond pads** and the **bond pad**-to-**lead** connections. The moulded insulator **encapsulates** the **die**, the **lead** inner portions, the thermal induction plate and the connections to form an **encapsulated package**. The thermal plate extends coextensive with the **encapsulated package**.

ADVANTAGE - Improved heat dissipative capacity and electrical performance. Conductive layers enable uniform power and ground supplies to be provided to circuitry formed on **die**, reduce **package lead** inductance, provide decoupling capacitances that reduce switching noise and crosstalk, and allow increased flexibility in placement of particular circuit components.

Dwg.1/8

L21 ANSWER 14 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1996-066680 [07] WPIX
DNN N1996-056156
TI Multi-**chip** semiconductor **package** - has insulating resin **protection** layer that is formed on **peripheral** end surface of mounting part where semiconductor **chip** is mounted.
DC U11
IN KIM, Y; SUN, Y
PA (SMSU) SAMSUNG ELECTRONICS CO LTD
CYC 2
PI JP 07326709 A 19951212 (199607)* 8p
KR 134647 B1 19980420 (200012)
ADT JP 07326709 A JP 1995-132006 19950530; KR 134647 B1 KR 1994-11812 19940530
PRAI KR 1994-11812 19940530
AB JP 07326709 A UPAB: 19960222
The **package** is provided with a non-conductive resin **protection** layer (90) that is formed on the **peripheral** end surface of a mounting part where a semiconductor **chip** is mounted, using a non-conductive adhesive agent. The **protection** layer encloses the **peripheral** of an adhesive agent (87) in order to prevent it to penetrate into a **bonding pad** (86) of a silicon substrate (80), and hides a metal pattern layer (84).
The silicon substrate is **electrically connected** to several internal **bonding pads** which are mounted on a **die** pad through the adhesive agent. Several external **bonding pad** is **electrically connected** by a wire (89) to a **lead** of a **lead** frame.
ADVANTAGE - Improves data storing capability of normal semiconductor component thus raising its integration density. Prevents metal pattern layer deformation due to external forceful stress. Reduces **package** size.
Dwg.5/8

L21 ANSWER 15 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1996-034310 [04] WPIX
DNN N1996-029122
TI Ball grid array type **IC die package** - has multiple second electric connections existing between **contact pads** provided at bottom surface and balls provided under **die package**.
DC U11
IN CHIA, C J; VARIOT, P
PA (LSIL-N) LSI LOGIC CORP
CYC 2
PI JP 07283341 A 19951027 (199604)* 6p
US 5563446 A 19961008 (199646) 7p
US 5789811 A 19980804 (199838)
US 5933710 A 19990803 (199937)
ADT JP 07283341 A JP 1995-10040 19950125; US 5563446 A US 1994-187238 19940125; US 5789811 A Cont of US 1994-187238 19940125, US 1996-725735 19961004; US 5933710 A Cont of US 1994-187238 19940125, Div ex US 1996-725735 19961004, US 1997-910608 19970813
FDT US 5789811 A Cont of US 5563446; US 5933710 A Cont of US 5563446, Div ex US 5789811

PRAI US 1994-187238 19940125; US 1996-725735 19961004; US 1997-910608 19970813
AB JP 07283341 A UPAB: 19960129
The **IC die package** (10) has **peripheral contact pads** (43) and **contact** balls provided at bottom surface. The first group of **contact pads** has multiple electrically conductive **leads**, each extended from **peripheral** part. The second group has multiple ball contacts (80,82) on the bottom.
Multiple first electric connections exists between each electrically conductive **lead** and each of first group **contact pads**. Multiple second electric connection exists between each ball contact and each of second group **contact pads** provided at bottom.
ADVANTAGE - Increases number of input and output connections of **die package**. Reduces size of **die package**.
Dwg.1/4

L21 ANSWER 16 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1995-302867 [39] WPIX
DNN N1995-229940
TI **IC** having clamp device preventing ESD damage to capacitors - Has diode formed in isolated P-type **chip** cell and formed of annular P-type plug at cell periphery and N-type circular plug at centre..
DC U12 U13
IN BEIGEL, D F; FEINDT, S L; KRIEGER, W A
PA (ANLG) ANALOG DEVICES INC
CYC 18
PI WO 9522842 A1 19950824 (199539)* EN 14p
RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
W: JP
US 5477078 A 19951219 (199605) 5p
EP 745275 A1 19961204 (199702) EN 14p
R: DE FR GB
US 5594266 A 19970114 (199709) 5p
EP 745275 A4 19970521 (199737)
JP 09509532 W 19970922 (199748) 12p
EP 745275 B1 20011017 (200169) EN
R: DE FR GB
DE 69523291 E 20011122 (200201)
ADT WO 9522842 A1 WO 1995-US2103 19950217; US 5477078 A Cont of US 1994-198856 19940218, US 1994-363384 19941223; EP 745275 A1 EP 1995-910306 19950217, WO 1995-US2103 19950217; US 5594266 A Cont of US 1994-198856 19940218, Div ex US 1994-363384 19941223, US 1995-546188 19951020; EP 745275 A4 EP 1995-910306 ; JP 09509532 W JP 1995-521963 19950217, WO 1995-US2103 19950217; EP 745275 B1 EP 1995-910306 19950217, WO 1995-US2103 19950217; DE 69523291 E DE 1995-623291 19950217, EP 1995-910306 19950217, WO 1995-US2103 19950217
FDT EP 745275 A1 Based on WO 9522842; US 5594266 A Div ex US 5477078; JP 09509532 W Based on WO 9522842; EP 745275 B1 Based on WO 9522842; DE 69523291 E Based on EP 745275, Based on WO 9522842
PRAI US 1994-198856 19940218; US 1994-363384 19941223; US 1995-546188 19951020
AB WO 9522842 A UPAB: 19951004
An electrostatic discharge **protective** clamp device (10) is formed in an isolated **chip** cell doped with a first, pref. P,

type dopant. Pref. the cell comprises a lightly doped P-type epitaxial layer (32) overlying a heavily doped P-type buried layer (30).

A P-type annular plug (34) at the cell periphery forms a diode anode. A circular N-type plug (42) at the cell centre forms the cathode. Pref. both plugs are formed in the epitaxial layer. Contacts (40,46) allow the diode to be connected to shunt electrostatic pulses from an external **bond pad** to a low impedance bus and prevent capacitor damage.

ADVANTAGE - Esp. suitable for use with metal-oxide-metal capacitors. Can deliver more than 2000 volt ESD **protection**.
Dwg.2/3

L21 ANSWER 17 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1995-060343 [08] WPIX
CR 1996-068357 [07]
DNC C1995-026877
TI Three-dimensional multi-**chip** array **package** - has master semiconductor device supporting and electrically interconnected with stacked array of subordinate semiconductor devices etc..
DC A85 L03
IN HSU, C
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI US 5380681 A 19950110 (199508)* 12p
ADT US 5380681 A US 1994-214990 19940321
PRAI US 1994-214990 19940321
AB US 5380681 A UPAB: 19960227
Fabricating a 3-D multichip array **package** having an **IC** master semiconductor device supporting and interconnected with a densely stacked array of subordinate **IC** semiconductor devices comprises: (a) fabricating interconnected **IC** elements **electrically connected** to **contact** terminal **pads** arranged in an inner **peripheral** row on a master semiconductor substrate to form a master device forming **lead** terminal pads on the master device arranged in an outer **peripheral** row and **electrically connected** to the inner row of **contact** terminal **pads** forming an insulating layer of an organic material over the surface of the master device; (b) etching openings over the **contact** terminal **pads** and the **lead** terminal pads; (c) depositing a barrier metal layer and an Au layer over the **contact** terminal **pads** fabricating interconnected **IC** elements that are **electrically connected** to **contact** terminal **pads** arranged in a **peripheral** row on subordinate semiconductor substrate to form subordinate **IC** semiconductor devices, the pattern of the **contact pad** terminals matching the pattern of the **contact pad** terminals on the master devices; (d) depositing an insulating layer of an organic material over the surfaces of each subordinate **IC** semiconductor devices; (e) etching control openings through each of the **contact** terminal **pads** and substrates of the subordinate semiconductor devices, the central openings of a size less than the size of the **contact** terminal **pads**; (f) depositing a thin conformed dielectric layer over the surfaces of the subordinate semiconductor devices and on the surfaces of the central openings; (g) anisotropically etching away the conformed dielectric layer on the surfaces of the subordinate semiconductor devices and the top edges of the dielectric layer in the central openings to a

depth sufficient to exposed edge surfaces of the **contact** terminal **pads**; (h) stacking the subordinate semiconductor devices on the master semiconductor devices with the central openings of the subordinate semiconductor devices aligned over the row of **contact** terminal **pads** on the master semiconductor device; and (i) filling the openings with a conductive material to electrically interconnect the subordinate semiconductor devices and the master semiconductor device.

USE - Used as a novel semiconductor device structure that embodies a 3-D multichip array interconnected and supported on a base semiconductor device substrate.

ADVANTAGE - Fabrication of the structure is easier and simpler to perform. The **package** is less expensive and is capable of higher yields. A higher level of microminiaturisation is possible. There is less power dissipation and less signal delay than comparable structures.
Dwg.14/14

L21 ANSWER 18 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1994-288930 [36] WPIX
CR 1999-091870 [08]; 1999-514376 [43]; 1999-514377 [43]; 1999-514378 [43]; 2001-011512 [02]
DNN N1994-227662 DNC C1994-131653
TI **Lead** frame for mounting semiconductor **integrated circuit chips** - has suspension **leads** for supporting **chip** loading **die** pad, with **leads** emanating radially from central portion of **lead** frame structure.
DC L03 U11
IN KAJIHARA, Y; KAWAI, S; MIYAKI, Y; NAITO, T; SUZUKI, H; SUZUKI, K; TSUBOSAKI, K
PA (HITA) HITACHI LTD; (HITA-N) HITACHI MICON SYSTEM KK; (HITA-N) HITACHI MICROCOMPUTER SYSTEM
CYC 3
PI JP 06216303 A 19940805 (199436)* 15p
US 5378656 A 19950103 (199507) 29p
US 5637913 A 19970610 (199729) 29p
KR 322825 B 20020318 (200264)
ADT JP 06216303 A JP 1993-65784 19930325; US 5378656 A US 1993-38684 19930329; US 5637913 A Div ex US 1993-38684 19930329, US 1994-311021 19940922; KR 322825 B Div ex KR 1993-4078 19930317, KR 2000-47727 20000818
PRAI JP 1992-320098 19921130; JP 1992-71116 19920327
AB JP 06216303 A UPAB: 20021007
The **lead** frame consists of two parts, inner **lead** part (5a) and outer **lead** part (5b). Plating layer is formed in inner **lead** region. A **chip** loading part (3) supported by a suspension **lead** (4) which emerge out radially. The external dimension of **die** pad is smaller than external dimension of semiconductor **chip** (2). The **chip** is loaded onto the **chip** loading part. The inner **leads** of the **lead** frame are bonded to terminals in electrode pad of the semiconductor **chip**. According to outer dimension of semiconductor **chip** , **leads** are chopped.

ADVANTAGE - Accommodates semiconductor **chip** of varied dimensions. Raises reflow crack tolerance of large scale **integrated circuit package**. Suits to low volume mixed dimension production environment.
Dwg.1/32

L21 ANSWER 19 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1993-378841 [48] WPIX
DNN N1993-292565
TI **Package** for energy detector esp. semiconductor IR detector - has body with recess located along periphery to align with detector **bonding pads** on assembly and detector **pads** wire **bonded** to **package pads** connected to external **package** contacts.
DC S03 U12
IN DES, JARDIN W F; NELSON, E T; OZIMEK, E J; RIVERA, L A; TARN, T; DESJARDIN, W F
PA (EAST) EASTMAN KODAK CO
CYC 5
PI EP 571907 A2 19931201 (199348)* EN 10p
R: DE FR GB
JP 06037338 A 19940210 (199411)
US 5349234 A 19940920 (199437) 7p
EP 571907 A3 19940216 (199518)
EP 571907 B1 19990804 (199935) EN
R: DE FR GB
DE 69325853 E 19990909 (199943)
ADT EP 571907 A2 EP 1993-108300 19930521; JP 06037338 A JP 1993-129209 19930531; US 5349234 A US 1992-890451 19920529; EP 571907 A3 EP 1993-108300 19930521; EP 571907 B1 EP 1993-108300 19930521; DE 69325853 E DE 1993-625853 19930521, EP 1993-108300 19930521
FDT DE 69325853 E Based on EP 571907
PRAI US 1992-890451 19920529
AB EP 571907 A UPAB: 19940120
The **package** includes a body with front and back sides, and an edge which defines at least one recess. The recess is located along the body periphery so that the body aligns with **bonding pads** on the energy detector upon **package** assembly. There are **bond pads** supported on the **package** body.
The **package** also has external contacts on the upper side which are **electrically connected** to the **bond pads**. Pref. wire **bonds** are used between the **bonding pads** on the detector and **package** body.
An adhesive tape, adapted to mechanically and thermally bond the energy detector and body together, may be sized to cover part of the back side of the body and not to cover the recess, and to cover all the detector except the **bonding pads**.
USE/ADVANTAGE - In cryogenic environment. Simplifies assembly whilst improving thermal dissipation from **chip**; reducing stress due to differential expansion between **chip** and **package** over wide range of temperatures.
Dwg.2/2

L21 ANSWER 20 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1991-060756 [09] WPIX
CR 1989-163099 [22]
DNN N1994-038701
TI Resin **encapsulated** semiconductor memory for single in-line **packages** - uses tabless **lead** frame with **bonding pads** arranged on **chip** sos that it can be applied to other types of **chip** also.
DC U11 U14
IN IWAI, H; KINOSHITA, Y; KOSHIBA, S; MIYAZAWA, K; MURANAKA, M; TAKAHASHI, Y

PA (HITA) HITACHI LTD; (HISC) HITACHI VLSI ENG CORP
CYC 3
PI JP 03008363 A 19910116 (199109)* 9p
US 5287000 A 19940215 (199407)B 32p
KR 154532 B1 19981015 (200027)
ADT JP 03008363 A JP 1989-143676 19890605; US 5287000 A Cont of US 1988-256862 19881012, Cont of US 1990-531313 19900531, CIP of US 1990-540484 19900619, US 1991-674969 19910326; KR 154532 B1 KR 1990-7758 19900529
FDT US 5287000 A JP 01107548, Cont of US 4934820
PRAI JP 1989-143676 19890605; JP 1987-264679 19871020
AB US 5287000 A UPAB: 19940329 ABEQ treated as Basic
The semiconductor device has a semiconductor pellet with a rectangular main surface on which two memory cell arrays and a **peripheral** circuit including a row address decoder circuit are formed. The memory cell arrays are arranged in line along the longer sides and the **peripheral** circuit between them.

Several **bonding pads** are disposed between the memory cell arrays and **electrically connected** with the row address decoder circuit which is located adjacent to the **bonding pads**. Further **bonding pads** are disposed on the main surface. A body comprised of resin has a surf ace vertical to the main surface of the semiconductor pellet. Several **leads** protrude out from the body from the vertical surface and extend in the body with ends situated near the **bonding pads**. The **bonding pads** are **electrically connected** with the ends of the **leads**.

USE/ADVANTAGE - Reduction in component size. Improved yield. Increased operation speed and heat dissipation. (First major country equivalent to JP3008363A)
Dwg.1/24
AB JP 03008363 A UPAB: 20000606
The semiconductor device has a semiconductor pellet with a rectangular main surface on which two memory cell arrays and a **peripheral** circuit including a row address decoder circuit are formed. The memory cell arrays are arranged in line along the longer sides and the **peripheral** circuit between them.

Several **bonding pads** are disposed between the memory cell arrays and **electrically connected** with the row address decoder circuit which is located adjacent to the **bonding pads**. Further **bonding pads** are disposed on the main surface. A body comprised of resin has a surf ace vertical to the main surface of the semiconductor pellet. Several **leads** protrude out from the body from the vertical surface and extend in the body with ends situated near the **bonding pads**. The **bonding pads** are **electrically connected** with the ends of the **leads**.

USE/ADVANTAGE - Reduction in component size. Improved yield. Increased operation speed and heat dissipation. (First major country equivalent to JP3008363A)
Dwg.3/3

L21 ANSWER 21 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1990-254721 [34] WPIX
DNN N1990-197328
TI **Lead**-frame for assembly of multiple HF semiconductor

**chips** - reduces magnitude and variability of bond-wire parasitic electrical characteristics by close decoupling earthing surface.

DC U11
IN TURINSKY, G
PA (ROBV) VEB ROBOTRON-ELTRN
CYC 1
PI DD 276950 A 19900314 (199034)*
ADT DD 276950 A DD 1988-321741 19881114
PRAI DD 1988-321741 19881114
AB DD 276950 A UPAB: 19930928
The **lead**-frame consists of a substrate (1) on which a conductive surface (8) has been formed. The **chips** (2) are attached to this surface and **electrically connected** to it. A **peripheral** frame (4) is provided with wire-**bond pads** (6). The conductive surface (8) is raised in the area between the **chips** and the pads to make its plane (11) approach closely and run parallel to the bond wires (7) which reach from the **chip**-pads (5) to the **lead**-frame **bond-pads** (6).

The raising of the surface (8) pref. is effected by using a profiled form (9) of the correct height which is **electrically connected** to the surface (8).

ADVANTAGE - Decoupling of all bond wires to a power-supply or other reference-level, reducing the noise-levels. All bond wires have similar electrical properties, esp. low AC-resistance and absence of reflections which allows use of high operating frequencies and better calculation and control of electrical properties of **package**. @
1/3@

L21 ANSWER 22 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1989-163099 [22] WPIX
CR 1991-060756 [09]
DNN N1990-156672 DNC C1989-072506
TI Resin **encapsulated** semiconductor memory for single in-line **packages** - uses tabless **lead** frame with **bonding pads** arranged on **chip** sos that it can be applied to other types of **chip** also.
DC U11 U14
IN IWAI, H; KINOSHITA, Y; KOSHIBA, S; MIYAZAWA, K; MURANAKA, M; TAKAHASHI, Y
PA (HISC) HITACHI CHO LSI ENG CO LTD; (HITA) HITACHI LTD; (HITA) HITACHI MFG CO; (HISC) HITACHI VLSI ENG CORP
CYC 3
PI JP 01107548 A 19890425 (198922)* 20p
US 4934820 A 19900619 (199027)
US 5287000 A 19940215 (199407)B 32p
KR 9706529 B1 19970429 (199940)
ADT JP 01107548 A JP 1987-264679 19871020; US 4934820 A US 1988-256862 19881012; US 5287000 A Cont of US 1988-256862 19881012, Cont of US 1990-531313 19900531, CIP of US 1990-540484 19900619, US 1991-674969 19910326; KR 9706529 B1 KR 1988-13310 19881012
FDT US 5287000 A JP 01107548, Cont of US 4934820
PRAI JP 1987-264679 19871020; JP 1989-143676 19890605
AB US 5287000 A UPAB: 19940329 ABEQ treated as Basic
The semiconductor device has a semiconductor pellet with a rectangular main surface on which two memory cell arrays and a **peripheral** circuit including a row address decoder circuit are formed. The memory cell arrays are arranged in line along the longer sides and the

**peripheral** circuit between them.
Several **bonding pads** are disposed between the memory cell arrays and **electrically connected** with the row address decoder circuit which is located adjacent to the **bonding pads**. Further **bonding pads** are disposed on the main surface. A body comprised of resin has a surf ace vertical to the main surface of the semiconductor pellet. Several **leads** protrude out from the body from the vertical surface and extend in the body with ends situated near the **bonding pads**. The **bonding pads** are **electrically connected** with the ends of the **leads**.
USE/ADVANTAGE - Reduction in component size. Improved yield. Increased operation speed and heat dissipation. (First major country equivalent to JP3008363A)
Dwg.1/24

AB JP 01107548 A UPAB: 20000606
The semiconductor device has a semiconductor pellet with a rectangular main surface on which two memory cell arrays and a **peripheral** circuit including a row address decoder circuit are formed. The memory cell arrays are arranged in line along the longer sides and the **peripheral** circuit between them.
Several **bonding pads** are disposed between the memory cell arrays and **electrically connected** with the row address decoder circuit which is located adjacent to the **bonding pads**. Further **bonding pads** are disposed on the main surface. A body comprised of resin has a surf ace vertical to the main surface of the semiconductor pellet. Several **leads** protrude out from the body from the vertical surface and extend in the body with ends situated near the **bonding pads**. The **bonding pads** are **electrically connected** with the ends of the **leads**.
USE/ADVANTAGE - Reduction in component size. Improved yield. Increased operation speed and heat dissipation. (First major country equivalent to JP3008363A)

L21 ANSWER 23 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1989-133013 [18] WPIX
CR 1989-056547 [08]; 1997-092942 [09]; 1998-318425 [28]; 1999-454585 [38]; 2002-201088 [25]
DNN N1993-045081
TI Resin moulded **package** for e.g. 4 mega bit DRAM in DIP structure - has **peripheral** circuitry and **bonding pads** in **integrated circuit** centre between two memory cell arrays, with **lead** frame inner **leads** extending over substrate surface and separated from it by insulator.
DC U11 U14
IN KANEDA, A; MITANI, M; MIYAZAWA, K; MURAKAMI, G; NAKAMURA, S; NISHI, K; OGUCHI, S; SAKUTA, T
PA (HITA) HITACHI LTD; (HITA) HITACHI MFG CO
CYC 3
PI JP 01076732 A 19890322 (198918)*
US 5184208 A 19930202 (199308)B 11p
US 5365113 A 19941115 (199445) 10p
US 5514905 A 19960507 (199624) 14p
US 5742101 A 19980421 (199823) 11p

KR 9613778 B1 19961010 (199928)
KR 9704216 B1 19970326 (199937)
ADT JP 01076732 A JP 1987-234654 19870917; US 5184208 A Cont of US 1988-212485 19880628, US 1991-640584 19910114; US 5365113 A Cont of US 1988-212485 19880628, Cont of US 1991-640584 19910114, US 1993-125 19930104; US 5514905 A Cont of US 1988-212485 19880628, Cont of US 1991-640584 19910114, Div ex US 1993-125 19930104, US 1994-329824 19941027; US 5742101 A Cont of US 1988-212485 19880628, Cont of US 1991-640584 19910114, Div ex US 1993-125 19930104, Div ex US 1994-329824 19941027, US 1995-458166 19950602; KR 9613778 B1 KR 1988-7311 19880617; KR 9704216 B1 Div ex KR 1988-7311 19880617, KR 1992-12675 19920716
FDT US 5184208 A JP 01007628; US 5365113 A JP 01007628, Cont of US 5184208; US 5514905 A JP 01007628, Cont of US 5184208, Div ex US 5365113; US 5742101 A Cont of US 5184208, Div ex US 5365113, Div ex US 5514905
PRAI JP 1987-234654 19870917; JP 1987-161333 19870630

L21 ANSWER 24 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1989-056547 [08] WPIX
CR 1989-133013 [18]; 1997-092942 [09]; 1998-318425 [28]; 1999-454585 [38]; 2002-201088 [25]
DNN N1993-045081
TI Resin moulded **package** for e.g. 4 mega bit DRAM in DIP structure - has **peripheral** circuitry and **bonding pads** in **integrated circuit** centre between two memory cell arrays, with **lead** frame inner **leads** extending over substrate surface and separated from it by insulator.
DC U11 U14
IN KANEDA, A; MITANI, M; MIYAZAWA, K; MURAKAMI, G; NAKAMURA, S; NISHI, K; OGUCHI, S; SAKUTA, T
PA (HITA) HITACHI LTD; (HITA) HITACHI MFG CO
CYC 3
PI JP 01007628 A 19890111 (198908)* 5p
US 5184208 A 19930202 (199308)B 11p
US 5365113 A 19941115 (199445) 10p
US 5514905 A 19960507 (199624) 14p
KR 9613778 B1 19961010 (199928)
KR 9704216 B1 19970326 (199937)
ADT JP 01007628 A JP 1987-161333 19870630; US 5184208 A Cont of US 1988-212485 19880628, US 1991-640584 19910114; US 5365113 A Cont of US 1988-212485 19880628, Cont of US 1991-640584 19910114, US 1993-125 19930104; US 5514905 A Cont of US 1988-212485 19880628, Cont of US 1991-640584 19910114, Div ex US 1993-125 19930104, US 1994-329824 19941027; KR 9613778 B1 KR 1988-7311 19880617; KR 9704216 B1 Div ex KR 1988-7311 19880617, KR 1992-12675 19920716
FDT US 5184208 A JP 01007628; US 5365113 A JP 01007628, Cont of US 5184208; US 5514905 A JP 01007628, Cont of US 5184208, Div ex US 5365113
PRAI JP 1987-161333 19870630; JP 1987-234654 19870917

L21 ANSWER 25 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1988-169447 [25] WPIX
DNN N1988-129576
TI Ceramic **package** for high frequency semiconductor devices - has parallel spaced-apart ground planes, inter-**lead** isolation and signal transmission lines formed over spacing layer.
DC U11 U14
IN EARLY, J M; NEGUS, K J; PHY, W S
PA (FAIH) FAIRCHILD SEMICONDUCTOR CORP

CYC 7
PI EP 272188 A 19880622 (198825)* EN 7p
R: DE FR GB IT NL
JP 63192262 A 19880809 (198837)
US 4839717 A 19890613 (198930) 6p
ADT EP 272188 A EP 1987-402884 19871217; JP 63192262 A JP 1987-317609 19871217; US 4839717 A US 1988-205040 19880607
PRAI US 1986-944499 19861219; US 1988-205040 19880607
AB EP 272188 A UPAB: 19930923
The **package** has a ceramic base with parallel faces with a **peripheral** edge between the faces. The first face includes a site for attacking a semiconductor device. It has an internal ground plane formed on the first of the faces and extending substantially from the attachment site to the **peripheral** edge. An external ground plane is formed on the second face and covers the entire area. A device **electrically connects** the internal ground plane and the external ground plane. A ceramic spacing layer is over the internal ground plane on the first face of the ceramic base.

A number of signal transmission lines are formed one the ceramic spacing layer. It has a ceramic isolation layer formed over the mermaic spacing layer and filling spaces between adjacent conductors. It has a cover layer. The attachment site is a **cavity** formed in the ceramic base.

USE - Silicon emitter coupled logic (ECL) and current mode logic (CMC) having operating frequencies in gigahertz range.
1/5

L21 ANSWER 26 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1987-145783 [21] WPIX
DNN N1990-207578 DNC C1987-060669
TI Semiconductor device with **lead** frame - has tab on which **chip** is bonded and inner **lead** with wide portion.
DC U11
PA (HITA) HITACHI LTD; (HITQ) HITACHI MICROCOMPUTER ENG LTD; (HITQ) HITACHI MICROCOMPUTER ENG CORP
CYC 3
PI JP 62081738 A 19870415 (198721)* 10p
US 4951120 A 19900821 (199036)B
KR 9500205 B1 19950111 (199644)
ADT JP 62081738 A JP 1985-221832 19851007; US 4951120 A US 1988-283842 19881213; KR 9500205 B1 KR 1986-7396 19860904
PRAI JP 1985-221832 19851007

L21 ANSWER 27 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1983-840234 [50] WPIX
DNN N1983-221444
TI Leadless PCB or **integrated circuit package** connector - has clamps depressing and keeping PCB in housing whose deformation from torque is cancelled.
DC U11 V04
IN ICHIMURA, Y
PA (NIAV) JAPAN AVIATION ELTRN IND LTD; (NIAV) NIPPON KOKU DENSHI KOGYO KK
CYC 6
PI EP 95745 A 19831207 (198350)* EN 27p
R: DE FR GB IT
JP 58206145 A 19831201 (198403)
JP 58206146 A 19831201 (198403)

US 4498720 A 19850212 (198509)
EP 95745 B 19861008 (198641) EN
R: DE FR GB IT
DE 3366809 G 19861113 (198647)
ADT EP 95745 A EP 1983-105246 19830526; JP 58206145 A JP 1982-87897 19820526; JP 58206146 A JP 1982-87898 19820526; US 4498720 A US 1983-496847 19830523
PRAI JP 1982-87897 19820526; JP 1982-87898 19820526
AB EP 95745 A UPAB: 19930925
The connector mounts a first PCB (4) having terminal pads (6) onto a second PCB (5) having conductor elements. The connector has a housing (11) with a number of contact elements (12) with a spring contact portion (13) at one end and a terminal pin portion (14) at the other end. Clamps (22) depress and keep the PCBs in the housing to establish pressure **contact** of terminal **pads** with the **contacts**. A lower portion (27) of the clamp engages with a bottom surface (112) of the housing.

An upper end (23) of the clamp, engages with and depresses the upper surface of the first PCB. The lower portion engages the bottom surface near an imaginary line on which the bottom surface intersects with a line of action of the pressure acting on the housing from each contact element. A torque due to this pressure and a clamping force acting on the housing are cancelled.
5/9

L21 ANSWER 28 OF 38 WPIX (C) 2002 THOMSON DERWENT
AN 1983-47270K [20] WPIX
DNN N1983-085134 DNC C1983-045863
TI Semiconductor device with leadless **chip** carrier - has heat sink connected to support plate serving as external terminal.
DC L03 U11
IN MIZUO, M
PA (FUIT) FUJITSU LTD
CYC 5
PI EP 78684 A 19830511 (198320)* EN 14p
R: DE FR GB
JP 58075859 A 19830507 (198324)
EP 78684 B 19880727 (198830) EN
R: DE FR GB
DE 3278844 G 19880901 (198836)
US 4910584 A 19900320 (199017)
ADT EP 78684 A EP 1982-305775 19821029; US 4910584 A US 1988-235814 19880823
PRAI JP 1981-173953 19811030
AB EP 78684 A UPAB: 19930925
Semiconductor device comprises a semiconductor **chip** (10) mounted on a major face of a support plate, with a cap (2,8) secured to the support to **encapsulate** the **chip**. The **peripheral** side surfaces of the device have no projecting conductive pins, but have conductive regions connected to terminals (11) of the **chip** for external connection. A conductive plate-form heat sink (21a) is attached to the other main face of the support plate and is **electrically connected** to another terminal of the **chip**, pref. via a hole (19a) extending through the support plate.

Pref. second electrically conductive plate-form heat sink (21b) is attached to the support plate (spaced from the first heat sink) and **electrically connected** to another terminal or the **chip**. The device is pref. arranged and connected in electrical

circuitry with other similar devices and the heat sinks are used as terminals for application of **chip** selecting signals. The **chip** is pref. a semiconductor memory **chip**.

The structure provides improved heat dissipation, allowing increased packing density, and reduces the length of connections for increased switching speed.

3B/5

L21 ANSWER 29 OF 38 JAPIO COPYRIGHT 2002 JPO
AN 2000-304836 JAPIO
TI HALL ELEMENT FOR **PERIPHERAL** OPPOSING TYPE HALL MOTOR AND **PERIPHERAL** OPPOSING TYPE HALL MOTOR
IN OKADA ICHIRO
PA ASAHI KASEI ELECTRONICS CO LTD
PI JP 2000304836 A 20001102 Heisei
AI JP 1999-111223 (JP11111223 Heisei) 19990419
PRAI JP 1999-111223 19990419
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To reduce noise generated in a magnetic field of a stator and increase an output voltage when a Hall element is mounted on a **peripheral** opposing type Hall motor.
SOLUTION: This Hall element for **peripheral** opposing type Hall motor which is molded is constituted in such a way that a Hall element pellet 12 is provided on a **die pad** and a **bonding pad** of the Hall element pellet 12 is **electrically connected** with a **lead** 11. In this **case**, the **die** pad provided with the Hall element pellet 12 is provided by deviating it from a central part of the Hall element **package** in the longitudinal direction.
COPYRIGHT: (C)2000,JPO

L21 ANSWER 30 OF 38 JAPIO COPYRIGHT 2002 JPO
AN 1995-183447 JAPIO
TI SEMICONDUCTOR DEVICE
IN MURAI NAOYUKI
PA NEC KYUSHU LTD
PI JP 07183447 A 19950721 Heisei
AI JP 1993-324971 (JP05324971 Heisei) 19931222
PRAI JP 1993-324971 19931222
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1995
AB PURPOSE: To reduce the thickness of a semiconductor device constituted of a semiconductor **chip**, an island, Au wires, and sealing resin, without deteriorating the reliability.
CONSTITUTION: An island suspension part 4 is subjected to a press working, and bent in a manner that an island part 2 is positioned above the **peripheral leads** 3. A semiconductor **chip** 1 is bonded to the lower surface of the island 2 in a manner that the face of a **bonding pad** 6 is up. The size of the island 2 is smaller than that of the semiconductor **chip** 1, and the **bonding pad** 6 is exposed from the periphery of the island 2. After that, the **bonding pad** 6 is **electrically connected** to **leads** 3 by using Au wires 5, and a **package** is completed by sealing with sealing resin 8.
COPYRIGHT: (C)1995,JPO

L21 ANSWER 31 OF 38 JAPIO COPYRIGHT 2002 JPO
AN 1992-103158 JAPIO

TI SEMICONDUCTOR **INTEGRATED CIRCUIT**
IN TSUTSUMI TOSHIYUKI
PA NEC CORP
PI JP 04103158 A 19920406 Heisei
AI JP 1990-221527 (JP02221527 Heisei) 19900823
PRAI JP 1990-221527 19900823
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1992
AB PURPOSE: To enable a semiconductor **integrated circuit** of this design to secure a bonding region larger than that of a conventional square **chip** by a method wherein the semiconductor **integrated circuit** is formed into a cross.
CONSTITUTION: The region of a semiconductor **integrated circuit** where an inner circuit is arranged is formed into the shape of a cross. That is, the semiconductor **integrated circuit** is composed of three regions, a region 1 where an inner circuit is provided, a second region 2 where the input/output circuit of an outer terminal and a control circuit are provided, and a region 3 where **pads bonded** to **package** terminals are provided.
The semiconductor **integrated circuit** is provided with a **lead** frame 4, a semiconductor **integrated circuit chip** 5, and a bonding wires 6 which **electrically connect** a semiconductor **integrated circuit chip** to **leads**. When all the sides are equal in length, the length of the **peripheral** part of the semiconductor circuit **chip** 5 is 1.2 times as large as that of a conventional **chip** equal to the **chip** 5 in area, so that a bonding region is enlarged and wiring can be increased in number.


L21 ANSWER 32 OF 38 JAPIO COPYRIGHT 2002 JPO
AN 1991-209852 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE
IN MITANI TSUNEO
PA HITACHI LTD
PI JP 03209852 A 19910912 Heisei
AI JP 1990-5077 (JP02005077 Heisei) 19900112
PRAI JP 1990-5077 19900112
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1991
AB PURPOSE: To surely prevent a dielectric breakdown from occurring in an inerlaminar insulting layer which isolates a connection pattern connected to an unused **lead** (NC **lead**) from a wiring of different potential by a method wherein a modifying pattern is provided between a **bonding pad** and a **peripheral** circuit in a wiring process if necessary.
CONSTITUTION: A connection pattern 8 not connected to any of **bonding pads** 2a and 2d and a circuit element 3 is provided between the pads 2a and 2b and the circuit element 3, and a modifying pattern 12 is provided between the **bonding pads** 2a and 2b and the connection pattern 8 and the circuit element 3 and the connection pattern 8 respectively in a following wiring process if necessary. A **bonding pad** 2 is **electrically connected** to the circuit element 8. By this setup, even if an NC **lead** is stored with charges, the NC **lead** is connected to a connection pattern, so that an interlaminar insulating film which isolates the connection pattern from a wiring of different potential can be surely **protected** against dielectric breakdown.

L21 ANSWER 33 OF 38 JAPIO COPYRIGHT 2002 JPO
AN 1991-169062 JAPIO
TI SEMICONDUCTOR DEVICE
IN GOTO SEIJI
PA NEC KYUSHU LTD
PI JP 03169062 A 19910722 Heisei
AI JP 1989-310161 (JP01310161 Heisei) 19891128
PRAI JP 1989-310161 19891128
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1991
AB PURPOSE: To reduce a **package** occupation area of a semiconductor device on a circuit board and to improve integration of a circuit board by stacking semiconductor **chips** solidly.
CONSTITUTION: A first semiconductor **chip** 1 is mounted on an island 5. An inner **lead** 6 provided on the periphery of the island 5 and a pad electrode 7 provided on the **peripheral** edge part of the semiconductor **chip** 1 are connected by a thin metal wire 4. Then, a second semiconductor **chip** 2 is mounted which has a bump 3 corresponding to a pad electrode 8 provided inside the pad electrode 7; the pad electrode 8 and the **bump** 3 are **bonded** by pressure; and the semiconductor **chip** 1 and the semiconductor **chip** 2 are **electrically connected**. Thereby, it is possible to reduce a **package** occupation area of a semiconductor device on a circuit board and to improve integration of a circuit board.


L21 ANSWER 34 OF 38 JAPIO COPYRIGHT 2002 JPO
AN 1990-090655 JAPIO
TI **PACKAGE** FOR SEMICONDUCTOR USE
IN SUZUKI KATSUHIKO
PA NEC CORP
PI JP 02090655 A 19900330 Heisei
AI JP 1988-245033 (JP63245033 Showa) 19880928
PRAI JP 1988-245033 19880928
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1990
AB PURPOSE: To reduce a continuity resistance and to adapt to the high-speed operation of a semiconductor device as well by a method wherein, in each layer of lower-stage, middle-stage and upper-stage metallized layers, which are printed on an insulating substrate and an insulating layer, the metallized layer is directly extended from a **bonding pad** to a **lead** connecting part and is led out directly to the exterior without the mediation of a through hole.
CONSTITUTION: A lower-stage metallized layer 3 consisting of tungsten or the like, which is arranged on the **peripheral** edge of an opening part of a ceramic substrate 1 having the opening part at its central part and is arranged toward the outer periphery of the substrate 1, is provied. Then, an insulating layer 12a is provided on the surface, from which the surface in the vicinity of the opening part and the vicinity of the outer periphery of the substrate 1 is excepted, of the layer 3 and a middle-stage metallized layer 11 is provided on the layer 12a in a way identical with a way of providing the layer 3. In the same way, an insulating layer 12b and an upper-stage metallized layer 4 are provided on the surface including the surface of the layer 11 and an insulating layer 12c is provided on the surface including the surface of the layer 4. A heat sink 10 with an element placing part 2 provided thereon is inserted

and fixed in the opening part, a semiconductor **chip** 14 is mounted on the placing part 2 and each metallized layer at each **bonding pad** part and electrodes of the **chip** 14 are **electrically connected** to each other.
COPYRIGHT: (C)1990,JPO&Japio

L21 ANSWER 35 OF 38 JAPIO COPYRIGHT 2002 JPO
AN 1990-086154 JAPIO
TI SEMICONDUCTOR DEVICE
IN UCHIYAMA HIROYUKI; OGUCHI SATOSHI
PA HITACHI LTD
PI JP 02086154 A 19900327 Heisei
AI JP 1988-236423 (JP63236423 Showa) 19880922
PRAI JP 1988-236423 19880922
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1990
AB PURPOSE: To realize miniaturization, and improve mounting density by dividing **leads** into two groups, stacking them at a specified interval so as not to come into contact with each other, and leading out the **leads** from a **package** in the above-mentioned state.
CONSTITUTION: **Leads** 12 are divided into two groups; these groups are stacked, via an insulating layer, at a specified interval so as not to come into contact with each other; a semiconductor **chip** 13 is fixed on a tab 11 and a part of **lead** 12a arranged on the same plane as the tab 11, via epoxy adhesive agent or the like; the **bonding pad** of the semiconductor **chip** 13 and the **leads** 12 are **electrically connected** by wires 14. The semiconductor **chip** 13 and its **peripheral** region are **encapsulated** by a **package** 15 composed of, e.g., epoxy resin, and from one side surface of the **package** 15, the **leads** 12a, 12b are led out in the state that a specified interval is kept.
COPYRIGHT: (C)1990,JPO&Japio

L21 ANSWER 36 OF 38 JAPIO COPYRIGHT 2002 JPO
AN 1989-171234 JAPIO
TI SEMICONDUCTOR DEVICE
IN KOMORO ATSUSHI
PA TEXAS INSTR JAPAN LTD
PI JP 01171234 A 19890706 Heisei
AI JP 1987-329079 (JP62329079 Showa) 19871225
PRAI JP 1987-329079 19871225
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1989
AB PURPOSE: To improve positional accuracy of a semiconductor **chip**, by close contacting external **leads** directly with side faces of the semiconductor **chip** in electrically insulated relation, and **electrically connecting** the external **leads** with electrodes on the semiconductor **chip**.
CONSTITUTION: Each external **lead** 34 whose outer periphery is coated with an insulative material 24 is close contacted directly with a pair of opposing side faces 22, 23 of a semiconductor **chip** 31 consisting of an active area 20 and a **peripheral** area 21. While such close contact between the external **leads** and the semiconductor **chip** is kept by a special-purpose jig, **bonding pads** 25 on the **chip** 31 are wire bonded with the top faces of the **leads** 34 by means of wires 33. The device as a whole is sealed with resin 35 by the transfer molding process or the like. Since the **leads** 34 are close contacted with the

side faces of the **chip** 31 in electrically insulated relation and they are connected with each other by wire bonding, there is no clearance between the **chip** 31 and the **leads** 34 and the size of the packaging structure is close to the outer diameter of the **chip** 31. Further, since the **leads** 34 are contacted directly with the **chip** side faces, it is possible to ensure satisfactory positional accuracy of the **chip** 31 in the **package**.


L21 ANSWER 37 OF 38 JAPIO COPYRIGHT 2002 JPO
AN 1989-007628 JAPIO
TI SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF
IN KANEDA AIZO; MITANI MASAO; NAKAMURA SHOZO; NISHI KUNIHIKO; MURAKAMI HAJIME
PA HITACHI LTD
PI JP 01007628 A 19890111 Heisei
AI JP 1987-161333 (JP62161333 Showa) 19870630
PRAI JP 1987-161333 19870630
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1989
AB PURPOSE: To house a large **chip** in a small **package**, to reduce thermal stress of a wire bonded section, to obtain a **lead** burying length and to decrease the influence of a mechanical stress at the time of forming **leads** by arraying a **bonding pad** substantially at the center of an LSI **chip** on a linear line in the longitudinal direction of a **chip**.
CONSTITUTION: A plurality of **bonding pads** 1 are provided on a rectangular LSI **chip** 5, **leads** 7 are radially arranged on the **peripheral** edge of the **chip** 5, and the pads 1 are **electrically connected** by wire bonding to one ends of the **leads** 7. The pads 1 of a semiconductor device having a resin sealing **package** 9 of such a structure are arrayed substantially at the center of the **chip** 5 on a linear line in the longitudinal direction of the **chip** 5. For example, the surface of the **chip** 5 except the pads 1 is covered with a heat resistant electric insulating film 10, the covered surface and the rear face of a **lead** frame 6 are bonded fixedly in such a manner that the pads 1 oppose the ends of the **leads** 7, and the pads 1 are wire bonded to the end surfaces of the **leads** 7.


L21 ANSWER 38 OF 38 JAPIO COPYRIGHT 2002 JPO
AN 1987-195147 JAPIO
TI RESIN-SEALED SEMICONDUCTOR DEVICE
IN TEZUKA IZUMI; SAKURAI SHUICHI; FUKUDA ROUROU
PA HITACHI LTD
HITACHI MICRO COMPUT ENG LTD
HITACHI TOBU SEMICONDUCTOR LTD
PI JP 62195147 A 19870827 Showa
AI JP 1986-35157 (JP61035157 Showa) 19860221
PRAI JP 1986-35157 19860221
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1987
AB PURPOSE: To eliminate disconnections attributable to the moving of Al-wirings under thermal stress originating in a sealing resin and thereby to improve the reliability of a semiconductor device by a method wherein electrodes or through- holes of very small dimensions are not allowed to be present in the periphery of the sealing resin where the quantity of thermal stress is the largest under a temperature cycling test.

CONSTITUTION: A semiconductor **chip** 16 provided with a final **protecting** film 15 is sealed in a resin 17 and fixed to a **lead** material tab 18. **Electrical connection** is established by a metal wire 21, made for example of gold, between **bonding pads** 19 exposed in the final **protecting** film 15 and inner **lead** sections 20 sealed in the resin 17. Disconnection is prevented in a temperature cycling test when no contact holes or through-holes are provided in a **chip peripheral** region II where thermal stress collects in the resin 17 or when contact holes and through-holes in the **chip peripheral** region II are made to be larger in dimension than contact holes and through-holes in a **chip** middle region I for example, by the quantity equivalent to the displacement of Al-wirings ascribable to heat stress in the sealing resin 17.

L25 ANSWER 1 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 2002-556818 [59] WPIX
DNN N2002-440733
TI **Package** for MMC flash memory has molding covering part of one substrate side leaving external connection pads exposed.
DC U11 U12
IN CHANG, C; HUANG, C; YU, K
PA (SILI-N) SILICONWARE PRECISION IND CO LTD; (CHAN-I) CHANG C; (HUAN-I) HUANG C; (YUKK-I) YU K
CYC 2
PI US 2002066947 A1 20020606 (200259)* 14p
TW 454287 A 20010911 (200259)
ADT US 2002066947 A1 US 2001-922254 20010803; TW 454287 A TW 2000-125978 20001206
PRAI TW 2000-125978 20001206
AB US2002066947 A UPAB: 20020916
NOVELTY - A substrate unit (410) has a first surface (412) containing a number of nodes (418) and **die** pads (416). A series of external nodes (420) are formed on the second side (414) of the substrate, being **electrically connected** to the first nodes. A multimedia **chip** (430) has an active surface (432) containing a number of **bonding pads** (436) and a back surface (434) adhered to the **die**-pads (416) of the substrate. Molding compound (470) **encapsulates** the multimedia **chip**, the first surface of the substrate and the **conductive wires** (438). The second surface of the substrate and the external nodes are left exposed.
USE - Multimedia **chip package** (MMC) consisting of an ASIC controller and a flash memory.
ADVANTAGE - Provides MMC packaging without the need for a cap and hence the manufacturing process is simplified and the **package** volume is reduced.
DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross sectional view of the MMC **package**.
Substrate 410
First surface 412
Second surface 414
First **die** pads 416
External nodes 420
Multimedia **chip** 430
Active surface 432
Back surface 434
**Bonding pads** 436
**Conductive wires** 438
Molding compound 470
Dwg.7/8

L25 ANSWER 2 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 2002-487535 [52] WPIX
DNN N2002-385184 DNC C2002-138459
TI Fabrication of a **chip** size **package** includes partially etching an upper layer of a metal plate to form redistributed **conductive lines**.
DC L03 U11
IN CHEN, A; CHEN, C; LAI, J; LIN, C; SU, S
PA (WALS-N) WALSIN ADVANCED ELECTRONICS LTD

CYC 1
PI TW 457662 A 20011001 (200252)*
ADT TW 457662 A TW 2000-122018 20001018
PRAI TW 2000-122018 20001018
AB TW 457662 A UPAB: 20020815
NOVELTY - Process for the fabrication of a **chip** size **package** includes partially etching the upper layer of a metal plate to form a plurality of redistributed **conductive lines** in which **conductive lines** are supported by the lower layer of the metal plate.
DETAILED DESCRIPTION - Fabrication of a **chip** size **package** comprises:
providing a **chip** in which the top side of each **chip** has a plurality of **bonding pads**;
providing a metal plate in which the metal plate is divided into an upper layer and a lower layer, and forming at least a placement region corresponding to at least an aforementioned **chip** on the surface of the upper layer in the metal plate;
partially etching the upper layer of the metal plate to form a plurality of redistributed **conductive lines** in which the **conductive lines** are supported by the lower layer of the metal plate;
joining the **chip** into the placement region on the upper layer of the metal plate, and **electrically connecting** to the **conductive lines**;
providing a bottom pad between the **chip** and the upper layer of the metal plate; and
removing the lower layer of the metal plate
USE - **Chip** size **package** manufacture.
ADVANTAGE - The present invention has the function of connecting with multiple pins and has a smaller thickness.
Dwg.1/1

L25 ANSWER 3 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 2002-424666 [45] WPIX
DNN N2002-333849 DNC C2002-120244
TI Stacked **chip** scale **package** includes stacked two **chips**, each having pair of opposite sides with **bonding pads** which are **electrically connected** to mounting pads using **conductive wires**.
DC L03 U11 V04
IN CHEN, J; WANG, S
PA (ADSE-N) ADVANCED SEMICONDUCTOR ENG INC
CYC 1
PI US 6365966 B1 20020402 (200245)* 11p
ADT US 6365966 B1 US 2000-632677 20000807
PRAI US 2000-632677 20000807
AB US 6365966 B UPAB: 20020717
NOVELTY - A stacked **chip** scale **package** includes stacked two **chips** above a substrate having mounting pads. Each **chip** has a pair of opposite sides having **bonding pads**. The pair of opposite edges of the first silicon **chip** is parallel to the pair of opposite edges of second silicon **chip** without **bonding pads**. The **bonding pads** are **electrically connected** to mounting pads using **conductive wires**.
DETAILED DESCRIPTION - A stacked **chip** scale **package**

comprises substrate having a surface with mounting pads positioned along lines close to four edges of the substrate (402). A first backside of a first **chip** is attached to first surface of the substrate so that the mounting pads (404) are located close to the edges of the first **chip**. A first active surface of the first **chip** includes first **bonding pads** (412) formed closed to a pair of short sides. A first backside of the **chip** is attached to first **chip** active surface such that the pair of sides having **bonding pads** is parallel to the pair of long sides of first **chip**. A second active surface of a second **chip** (410) includes second **bonding pads** formed close to the pair of sides having **bonding pads**. The second **chip** has smaller length and width than the dimension of the short sides of the first **chip**. The second **chip** has a pair of sides having **bond pad** and pair of sides free from **bonding pads**. The first **bonding pads** and corresponding mounting pads are **electrically connected** to pair of short sides by **conductive wires** (434). The second **bonding pads** and corresponding mounting pads are **electrically connected** to pair of long sides by **conductive wires**. The first **chip** on the first surface, second **chip**, mounting pads, and **conductive wires** are enclosed in molding compound.

USE - For use in packaging semiconductor **chips**.

ADVANTAGE - The **package** reduces **package** thickness and prevents any short-circuiting between **conductive wires**.

DESCRIPTION OF DRAWING(S) - The drawing shows a schematic top view of the inventive stacked **chip** scale **package**.

Substrate 402

Mounting pads 404

Second **chip** 410

**Bonding pads** 412

**Conductive wires** 434

Dwg.6/9

L25 ANSWER 4 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 2002-400943 [43] WPIX
TI Wire bonding structure between semiconductor **chip** and substrate, semiconductor **package** using the same and method for manufacturing semiconductor **package**..
DC U11
IN HA, S H; KO, S G; PARK, Y G; SIM, I G
PA (AMKO-N) AMKOR TECHNOLOGY KOREA INC
CYC 1
PI KR 2001111659 A 20011220 (200243)* 1p
ADT KR 2001111659 A KR 2000-32214 20000612
PRAI KR 2000-32214 20000612
AB KR2001111659 A UPAB: 20020709

NOVELTY - A wire bonding structure between a semiconductor **chip** and a substrate, a semiconductor **package** using the same and the method for manufacturing the semiconductor **package** are provided to facilitate an inter-connection of a plurality of semiconductor **chips** having the sizes different to each other by forming a loop of a **conductive wire** connected and formed to an input/output pad of the respective semiconductor **chip** so that the loop height of the **conductive wire** is lower than

an upper plane height of the semiconductor **chip**.
DETAILED DESCRIPTION - In a wire bonding structure between a semiconductor **chip** and a substrate and a semiconductor **package**(101) using the same, a substrate(1) having a plurality of circuit patterns formed thereon is **packaged** in a mother board. The first semiconductor **chip**(10) of which inner fringe has a plurality of input/output **pads**(10a) is **bonded** to the center of an upper plane of the substrate with an adhesive means(50). The second semiconductor **chip**(20) of which upper plane fringe has a plurality of input/output **pads** is **bonded** on an upper plane of the first semiconductor **chip** with the adhesive means. Bond fingers(3) of the substrate and the input/output pads of the first and second semiconductor **chips** are **electrically connected** to each other. A plurality of **conductive wires** connects the bond fingers with the input/output pad electrically. A loop height(LH) formed between the semiconductor **chip** and the substrate is equal to the upper plane height of the semiconductor **chip**.
Dwg.1/10

L25 ANSWER 5 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 2002-356732 [39] WPIX
DNN N2002-280495
TI Stacked **die package** structure with BGA structure for packaging **integrated circuit**, has mold which covers carrier upper face for **capsule** accommodation of spacer, **die** and cementing layer.
DC U11 U14
PA (SEKI-N) SEKIPIN PRECISION IND CO LTD
CYC 1
PI JP 2002057272 A 20020222 (200239)* 37p
ADT JP 2002057272 A JP 2000-237651 20000804
PRAI JP 2000-237651 20000804
AB JP2002057272 A UPAB: 20020621
NOVELTY - The **dies** (206,208) are formed on the upper face (201) of a carrier (202) through a spacer (220). A cementing layer (204) is provided between the spacer and **die**, **die** and carrier. Each **bonding pad** (222) and the carrier of a **die** are **electrically connected** by **conductive wire** (210). A mold (214) is formed to cover the upper face of a carrier for accommodation of spacer, **die** and cementing layer.
USE - Stacked **die package** provided with ball grid array (BGA) structure for packaging **integrated circuit** (**IC**).
ADVANTAGE - The stacked **die package** structure where the **die** of the almost same size which has a **bonding pad** on a periphery is accumulated within one **package** is provided.
DESCRIPTION OF DRAWING(S) - The figure shows top and sectional views of the stacked **die package** structure.
Upper face of carrier 201
Carrier 202
Under surface of carrier 203
Cementing layer 204
**Die** 206,208
**Conductive wire** 210

Mold 214
Spacer 220
**Bonding pad** 222
Dwg.4/9

L25 ANSWER 6 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 2002-162619 [21] WPIX
DNN N2002-124005
TI **Integrated circuit** packaging structure for memory device has **bonding pads** formed on top of each **dice** attached to bottom surface of circuit board, such that **bonding pads** are registered in aperture formed in PCB.
DC U11 U14
IN SHEN, M
PA (CTSC-N) CTS COMPUTER TECHNOLOGY SYSTEM CORP
CYC 1
PI US 6225691 B1 20010501 (200221)* 7p
ADT US 6225691 B1 US 1999-346742 19990702
PRAI US 1999-346742 19990702
AB US 6225691 B UPAB: 20020403
NOVELTY - **Integrated circuit** packaging structure has **bonding pads electrically connected** to corresponding electrical traces formed at top surface of printed circuit board (PCB). **Bonding pads** formed on upper surface of each **dice** are attached to bottom surface of PCB, such that **bonding pads** are registered in aperture formed in PCB. **Conductive wires** interconnect **bonding pads** of **dice** and PCB through aperture.
USE - For packaging **integrated circuits** such as memory devices.
ADVANTAGE - The **integrated circuit** packaging structure can **encapsulate** two or four memory **chips** into single **package** and thus enlarge the memory capacity, without increasing the size of the **package** and number of pins. The packaging structure can effectively promote the efficiency of a memory **IC**, and inner space of the **package** can be effectively used.
DESCRIPTION OF DRAWING(S) - The drawing shows a cross sectional view of the memory **chip package**.
Dwg.1B/4

L25 ANSWER 7 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 2002-039058 [05] WPIX
TI Semiconductor **package** having hang over type **chip** stack structure and using substrate with supporting post.
DC U11
IN PARK, Y G
PA (AMKO-N) AMKOR TECHNOLOGY KOREA INC
CYC 1
PI KR 2001055041 A 20010702 (200205)* 1p
ADT KR 2001055041 A KR 1999-56102 19991209
PRAI KR 1999-56102 19991209
AB KR2001055041 A UPAB: 20020123
NOVELTY - A semiconductor **package** having a hang over type **chip** stack structure and using a substrate with a supporting post is provided to permit a wire bonding between an upper **chip** and the substrate and further to improve allowance for **chip**

selection.

DETAILED DESCRIPTION - The **package** includes the substrate, which has a **chip**-mounting area(8), a circuit pattern(12), and the supporting posts(4) arranged in two rows on the **chip**-mounting area(8). The **package** further has at least two stacked semiconductor **chips**(2,2a) of a rectangular type. The first **chip**(2) is mounted on the **chip**-mounting area(8) between the rows of the supporting posts(4), and the second **chip**(2a) is mounted on the first **chip**(2). Each **chip**(2,2a) has the first opposite edges near which **bond pads**(3,3a) are formed and the second opposite edges without the **bond pads**. The **chips**(2,2a) cross each other so that the **bond pads**(3a) of the second **chip**(2a) are disposed over the second opposite edges of the first **chip**(2). In addition, the second opposite edges of the second **chip**(2a) are supported by the supporting posts(4). The **bond pads**(3,3a) of each **chip**(2,2a) are **electrically connected** to the circuit pattern(12) of the substrate by **conductive wires**, and external terminals are coupled to the circuit pattern(12).

Dwg.1/10

L25 ANSWER 8 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 2001-473844 [51] WPIX
TI Method for manufacturing **chip**-on-board **package**.
DC U11
IN NOH, G Y
PA (SMSU) SAMSUNG ELECTRONICS CO LTD
CYC 1
PI KR 2001010131 A 20010205 (200151)* 1p
ADT KR 2001010131 A KR 1999-28848 19990716
PRAI KR 1999-28848 19990716
AB KR2001010131 A UPAB: 20010910

NOVELTY - A method for manufacturing a **chip**-on-board **package** is provided to reduce the manufacturing cost and time, by forming a dam in a printed circuit board in a process for forming an **encapsulating** unit.

DETAILED DESCRIPTION - Adhesive(120) is put on a **chip**-mounted region(118) of a surface of a printed circuit board(110) having a plurality of circuit patterns(112) and the **chip**-mounted region. A semiconductor **chip**(130) is adhered to an upper surface of the adhesive, so that the printed circuit board is interconnected with the semiconductor **chip**. One end of a **conductive wire**(140) is bonded to a plurality of **bonding pads** formed on a side of the semiconductor **chip** and the other end of the **conductive wire** is bonded to ends of the circuit patterns, so that the semiconductor **chip** is **electrically connected** to the printed circuit board. A coating resin having a viscosity is applied along an edge of the printed circuit board at a predetermined location of the printed circuit board which is separated and formed at the outside of the **conductive wire** by a predetermined interval, and is hardened for several tens of seconds to form a dam(150) of a predetermined height. After the coating resin having a viscosity is filled in the dam to **encapsulate** the semiconductor **chip**, the **conductive wire** and a predetermined portion of the circuit patterns to which the **conductive wire** is connected, the coating resin is

hardened to form an **encapsulating** unit.
Dwg.1/10

L25 ANSWER 9 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 2001-430604 [46] WPIX
TI **Wafer** level **chip** scale **package** having via holes and manufacturing method thereof.
DC U11
IN MUN, H J
PA (SMSU) SAMSUNG ELECTRONICS CO LTD
CYC 1
PI KR 2001001159 A 20010105 (200146)* 1p
ADT KR 2001001159 A KR 1999-20204 19990602
PRAI KR 1999-20204 19990602
AB KR2001001159 A UPAB: 20010815
NOVELTY - A **wafer** level **chip** scale **package**, as well as a manufacturing method thereof, is provided to permit a direct disposition of solder balls on a bottom surface of a **chip** through via holes formed at a **wafer** level.
DETAILED DESCRIPTION - A plurality of via holes is formed along scribe lines in a **wafer**. Each via hole makes an electrical path by a **conductive line**(120) formed therein. The **conductive lines**(120) in the via holes are **electrically connected** to **bonding pads** (112) on an active surface(114) of a semiconductor **chip**(110) with metallic wiring(140), and further to ball pads on a bottom surface(116) of the **chip**(110). After the **chips**(110) constituting the **wafer** are individually separated by a **wafer** sawing process, solder balls(150) are formed respectively on the ball pads of each **chip**(110). In addition, overall surfaces of the **chip**(110), except the ball pads, are sealed with **encapsulant**(130).
Dwg.1/10

L25 ANSWER 10 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 2001-272527 [28] WPIX
DNN N2001-194581
TI Ball grid array packaging device and the manufacturing process of the same - with the characteristics of low cost and high heat dissipation efficiency.
DC U11
IN HE, T; HUANG, J; HER, T; HUANG, C
PA (SILI-N) SILICONWARE PRECISION IND CO LTD; (HERT-I) HER T; (HUAN-I) HUANG C
CYC 2
PI TW 415054 A 20001211 (200128)*
US 2002000656 A1 20020103 (200207)#
ADT TW 415054 A TW 1999-117378 19991008; US 2002000656 A1 US 1999-451135 19991130
PRAI TW 1999-117378 19991008; US 1999-451135 19991130
AB TW 415054 A UPAB: 20010522
NOVELTY - The invention relates to a ball grid array (BGA) packaging device and the manufacturingprocess of the same. At first, a heat dissipation substrate, which has the first surface and the second surface, is provided. The isolation layer and the copper foil are then stacked and matched on the second surface sequentially. The copper foil is patterned to form multiple conductive traces. The solder resist is coated on the

surfaces of the conductive traces and the isolation layer, in which part surface of the conductive traces is exposed and at least multiple bonding fingers and multiple ball pads are formed. A conducting hole, which is formed at the center of the heat dissipation substrate and the isolation layer, punches through the heat dissipation substrate and the isolation layer. A **chip**, in which the active surface is bonded with the first surface, is provided. There are multiple **conductive lines** are **electrically connected** with the **bonding pad** and **bonding** finger on the active surface individually by going through the conductive hole. The packaging material is used to cover the **chip**, the **conductive wire** and the bonding finger, and the solder ball is individually bonded to the ball pad.
Dwg.1/1

L25 ANSWER 11 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 2001-218086 [22] WPIX
DNN N2001-155477 DNC C2001-065033
TI Manufacture of **package** board for carrying a low pin count **IC chip**.
DC A85 L03 U11
IN CHENG, D C H
PA (CHEN-I) CHENG D C H
CYC 1
PI US 2001000156 A1 20010405 (200122)* 10p
ADT US 2001000156 A1 Div ex US 1999-325364 19990604, US 2000-725634 20001129
PRAI US 1999-325364 19990604; US 2000-725634 20001129
AB US2001000156 A UPAB: 20010421
NOVELTY - A method for forming a **package** board for carrying a low pin count **IC chip**. A hard resin substrate board is provided. through vias are formed in locations where ball grid pads are needed.

DETAILED DESCRIPTION - A conductive layer that also covers the vias is attached to the surface of the board using glue material. The conductive layer is patterned to form a **conductive line** layer. Ball grid pad regions on the **conductive line** layer are located above the vias. A soldering mask that covers a portion of the **conductive line** layer is formed. An electroplated layer is formed over the **bonding pad** regions.

USE - **Package** board for carrying a low pin count **IC chip**.

ADVANTAGE - **Package** provides support to the **IC chip** but serves as medium for **electrical connection** between devices and gives mechanical **protection**.

DESCRIPTION OF DRAWING(S) - substrate board 200
glue layer 206
conductive layer 208
ball grid pad regions 210
solder mask 212
**bonding pad** regions 214
Dwg.2/3

L25 ANSWER 12 OF 12 WPIX (C) 2002 THOMSON DERWENT
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TI Printed circuit board for mounting electronic component e.g. semiconductor **package** - has two semiconductor **chips** fixed to each other such that electrode in first semiconductor **chip** opposes electrode in second semiconductor **chip** in contact state with electrically conductive protrusions.

DC U11 U14 V04
PA (TOSH-N) TOSHIBA COMPUTER ENG KK; (TOKE) TOSHIBA KK
CYC 1
PI JP 09330952 A 19971222 (199810)* 7p
ADT JP 09330952 A JP 1996-152357 19960613
PRAI JP 1996-152357 19960613

AB JP 09330952 A UPAB: 19980316
The printed circuit board includes a printed circuit (12) on which a conductor pattern containing **contact pads** (16) is formed. Several electrodes (20) are formed on the electrode formation surfaces (22). Semiconductor **chips** (18a,18b) are mounted in a lamination state on the printed circuit. The semiconductor **chip** of the second layer is fixed opposing the semiconductor **chip** of the first layer on the printed circuit such that the back surface (24) of the second semiconductor **chip** is placed on the top.

A pair of electrically conductive protrusions (34) corresponding to the electrodes of the semiconductor **chip** of the first layer, are **electrically connected** to the **contact pad** of the printed circuit via electrically **conductive wires** (32). The electrode formation surface in the first semiconductor **chip** opposes the electrode formation surface in the second semiconductor **chip**. Each electrode in the second semiconductor **chip** oppose the corresponding electrode in the first semiconductor **chip** in a state wherein it contacts the protrusions.

ADVANTAGE - Semiconductor **chips** can be easily mounted at low cost. Does not need to apply special wire **protection** process.

Dwg.1/8